

# Millimeter-wave CMOS Antennas and RFIC Parameter Extraction for Vehicular Applications

Felix Gutierrez, Jr., Theodore S. Rappaport, and James Murdock

The Wireless Networking and Communications Group (WNCG)

Department of Electrical and Computer Engineering, The University of Texas at Austin

[felixgutierrez, wireless, jmurdock]@mail.utexas.edu

**Abstract**—This paper reviews recent developments in vehicular radar at 60 GHz and above, with a focus on low cost integrated antennas. We investigate a number of radar and communication antenna systems that can be made inexpensively and in large volumes using standard CMOS semiconductor fabrication methods. As shown here, the electromagnetic characteristics of low cost CMOS processes are often not well understood when applied to mmWave and THz RF applications. Here, we describe several methodologies and measured results to understand electromagnetic behavior of integrated circuits and on-chip antenna performance in a 180nm CMOS process up to 67 GHz. By gaining understanding of the electrical characteristics of older, lower cost semiconductor CMOS processes, it becomes possible to design mmWave on-chip antennas and other passive devices at extremely low cost and with great reliability.

**Index Terms**—60 GHz, 77 GHz, millimeter-wave, on-chip antenna, RFIC, CMOS, vehicle radar

## I. INTRODUCTION

Vehicular radar and emerging WPANs at 60-90 GHz demand high gain, small beamwidth, steerable antennas to transmit and receive data. Antennas that meet these criteria will enable numerous applications, such as “information show-ers” that provide high speed data and information content to consumers or vehicles, as well as vehicular radars that anticipate hazards and improve driver safety. As seen in Figure 1, vehicles are being equipped with millimeter-wave (mmWave) frequency radar to help drivers avoid collisions in all directions.

As wireless carrier frequencies continue to increase due to massive spectrum allocations at 60 GHz and above, the devices and antennas needed to transmit information become smaller, a trend that will continue [1, 2]. Antenna sizes that transmit these mmWave frequencies are a few millimeters and comparable to the sizes of integrated circuits (ICs). Soon, it will be economical to integrate antennas with their feeding circuits onto a complete system-on-chip (SoC) transceiver. To design reliable devices, the properties of an integrated circuit must be well understood, as circuit behavior is frequency dependent. Unfortunately, semiconductor manufacturers and practitioners often have limited knowledge about their own semiconductor process at mmWave or terahertz (THz) frequencies despite the fact that low cost, mature CMOS processes offer the lowest cost per chip for mass consumer markets (such as the vehicular industry or the portable laptop/cellphone market). This paper explores new ideas in vehicular electronics using integrated on-chip antennas and demonstrates how to

measure and model electromagnetic properties of integrated circuits (such as permittivity, conductivity, loss tangent) at mmWave frequencies. By quantifying the electrical properties, novel devices and antennas can be successfully designed and constructed on inexpensive, older silicon processes.

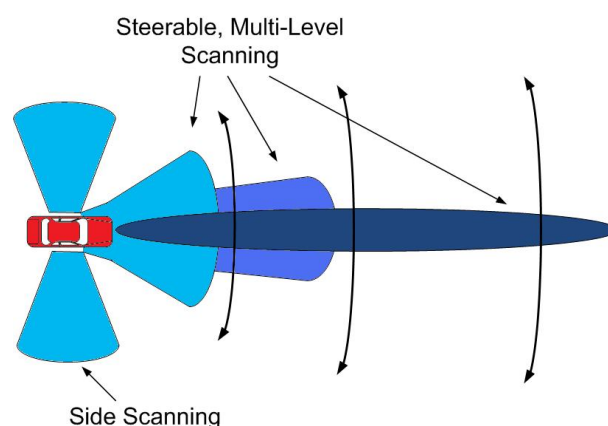


Fig. 1. Next generation vehicles will rely on arrays of antennas to provide high gain, steerable beams [3]. These beams will enhance driver safety with collision avoidance and provide passengers with high-speed data content.

## II. STATE OF MMWAVE VEHICLE RADAR

Safety and comfort are important priorities for car manufacturers. Providing additional features such as “blind-spot” awareness and cruise control radar are attractive options [3]. High gain antennas are needed especially for LRR (Long Range Radar) at 76 - 77 GHz to overcome the larger path loss compared to 24 GHz, which is used for short-range vehicular radar [3]. A tight steerable antenna beamwidth is also needed to help differentiate closely spaced distant objects. An array of multiple antennas not only satisfies this high gain requirement but allows beamsteering by phasing the antennas appropriately. 77 GHz is attractive since the high frequency allows smaller antennas to be arranged in a tighter form factor, and tight beamwidths can be achieved.

The idea of integrating these small antennas directly into the IC is very attractive and considerably lowers the manufacturing cost. The drawback is the extremely low radiation efficiency (typically less than 10%) [1, 4] due to the lossy silicon substrate. Dielectric lenses and slabs as seen in [5–10] are used to help focus and steer beams, however these use specialized post-processing fabrication techniques that require

additional dielectric materials to be created and placed near the antenna/chip, which adds to manufacturing costs.

Nagasaku, [5], created a 77 GHz radar sensor using Gallium Arsenide (GaAs) p-HEMT technology with an on-chip patch antenna. A dielectric dome-shaped resin lens was placed exterior to the chip package and boosted gains by 11dB. The overall antenna gain with package and lens was 8 dBi and package consumed an area of 6.5 mm x 6 mm.

Babakhani, [6, 7], used four integrated dipole antennas on a SiGe BiCMOS process. Since 95% of radiated energy was lost through substrate coupling, the authors used a hemispherical dielectric lens with a similar dielectric permittivity to the substrate to channel energy from surface modes into useful radiation. This lens was attached to the backside of the chip. The peak measured antenna gain for the array was 2 dBi.

Weng, [8], created a 77 GHz frequency modulation continuous-wave (FMCW) radar front end and used a linear array of patch-subarrays to feed a cylindrical lens. The lens increased antenna gains by 9 dB. As noted by Cheng [9], FMCW radar is usually employed in vehicular radar since target distance is found by “counting the difference frequency between transmitting signal and its echo.” FMCW is desirable since ranging error is not dependent on fluctuations of the target’s radar cross section (RCS). In Cheng [9], a lens antenna is fed by a horn antenna located at the lens focal point. The horn antenna is fed by a microstrip patch antenna. The peak antenna gain of the entire system was 28.5 dBi with a half-power beam width of about 2.5°.

Menzel, [11], also implemented a 77 GHz FMCW radar sensor that used a “folded reflector-type antenna” that consisted of a printed slot array. The diameter of the large antenna array measured 100 mm and was 25 mm thick on a printed circuit board. This large array produced 35 dBi gain.

Matsuzawa, [10], constructed a leaky wave antenna and used a movable dielectric slab to steer the beam. Actuators were used to change the distance between the dielectric and the antenna. The device was optimized for 76 GHz, and the peak antenna gain was 12.3 dBi.

More specialized techniques have been used to try to improve antenna gains and radiation efficiencies. By suspending the antenna in air over a high dielectric constant substrate, Lee, [12], created a 77 GHz CPW-fed patch antenna with a simulated radiation efficiency of 94%. The antenna was mechanically supported by posts and hovered 200  $\mu\text{m}$  above the substrate surface. The area of the patch was 1.7 mm x 1.7 mm and had a 9 GHz bandwidth. Antenna gain was 9 dBi. Gardner, [13], used a custom-built air-spaced wideband microstrip antenna array with a gain of 15.5 dBi and a 25% bandwidth.

Shino, [14], used a packaging material (ceramic) to construct a linear polarized antenna array. These antennas were composed of a “laminated waveguide and rectangular resonator” to form an aperture array. A 2x12 and 4x12 array were created with overall antenna gains of about 15-17 dBi and beamwidths of 25° - 40°.

Both Montusclat, [15], and Morschbach, [16], investigated how integrated antennas behave on a non-standard less lossy substrate, HR (High Resistivity) silicon. HR silicon is ion-

implanted to reduce substrate conductivity and reduce energy loss. Montusclat used a 500  $\mu\text{m}$  substrate thickness and constructed a half-wave dipole antenna to operate at 40 GHz. The antenna gain was -2 dBi, 6dB better than the same antenna in standard bulk substrate. Morschbach created two separate antenna array designs at 80 GHz operation. One design consisted of a 1-D series fed antenna with 10 elements, and the 2nd design was a 2-D array of patch antennas. The 1-D antenna had 6.2 dBi gain with a simulated radiation efficiency of 22.93%. The 2-D design had 10 dBi gain with a simulated radiation efficiency of 53.9%.

What was once only possible in costly RF-optimized semiconductor technologies such as Silicon Germanium (SiGe) or Gallium Arsenide (GaAs) can now be achieved in inexpensive digital CMOS technology. The possibility of fabricating on CMOS offers significant cost savings. Several researchers such as Yao, [17], have created CMOS wireless RFICs at millimeter-wave frequencies such as 60 GHz and 77 GHz.

### III. SEMICONDUCTOR FABRICATION TECHNOLOGIES

Reducing transistor size allows higher frequencies and operation in the mmWave, and even THz regime [18]. However, as CMOS fabrication techniques use smaller transistor gates (e.g. 32 nm process), the price of fabrication increases. The cost of photomasks used to create ICs continues to increase for each new process [19]. The cost of building masks has increased by 200X from the 500 nm process of 2003 to the 65 nm process. Also, the doping concentration profiles in silicon have increased from 10  $\Omega\text{cm}$  in 180 nm CMOS to 0.1  $\Omega\text{cm}$  for newer CMOS processes. This higher substrate conductivity increases substrate losses in the form of eddy currents for inductors and on-chip antennas [19]. Therefore, older CMOS processes actually perform better for analog/RF and antenna applications at mmWave frequencies due to smaller, although still substantial, substrate loss.

As stated in [19], analog wafer manufacturing is one to two technology “nodes” behind cutting-edge digital logic processes. This delay translates to using older fabs, process equipment, and materials to create analog/RF devices, which reduces technical problems since new processes are able to mature for RFIC use. Today, digital CMOS ICs are being mass-produced using 45 nm processes and current research is developing the 32 nm process.

### IV. PROTOTYPE PHASED ARRAY FOR COLLISION DETECTION AND MATERIAL PARAMETER EXTRACTION

Highly directional, steerable beams can be realized by phasing several CMOS chips with integrated antennas on a printed circuit board (PCB) as seen in Figure 2. The low cost of CMOS creates incentive to use CMOS integrated antennas in a phased array for vehicular radars and communication systems. Emerging standards for WPANs will take beamforming into account and standards for beamforming will emerge much like error correction codes today [20]. The high-definition “information showers” enabled by these standards and applications will therefore be much cheaper with arrays constructed of on-chip versus off-chip antennas [1]. Frequency Selective Surfaces (FSS) also offer promise for future low cost

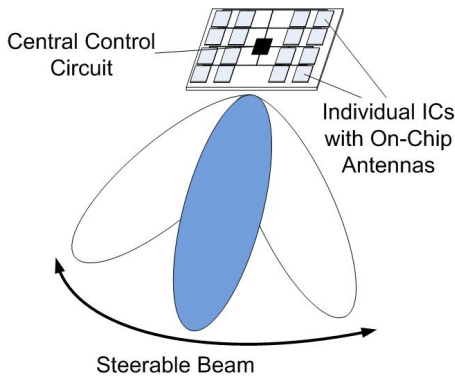


Fig. 2. Example phased array of mmWave IC antennas on PCB to create a highly directional and steerable beam. Applications include radar and high speed communications such as “information showers.”

on-chip antennas [21].

The individual ICs of the phased array can be constructed of several dozen materials [2], and designing and simulating mmWave communication or vehicular radar systems require accurate knowledge of their electromagnetic properties. All materials within the fabricated IC must be understood geometrically (length, thickness, etc.), and electrically (resistance, conductance, permittivity, etc.). These material parameters are frequency dependent, thus test chips must be initially constructed to measure and extract these values at mmWave and higher frequencies, especially if the foundry does not have these data for reliable circuit modeling.

#### A. On-Chip Building Block

Test chips at the University of Texas at Austin were fabricated on a low cost 180 nm standard CMOS process. Figure 3 shows a microscope image of one test chip, which contains an array of transmission lines that allow extraction of electrical properties with measurement. A dipole and Yagi antenna were also fabricated on the chip, as seen on the left.

A wafer probe station with Ground-Signal-Ground (GSG) probe tips was used to measure the IC with a Vector Network Analyzer (VNA) up to 67 GHz [1]. The response of the device under test (DUT) can be represented as a matrix of S-Parameters, and electrical properties can be extracted from S-Parameters. Figure 4 shows the  $S_{11}$  measurement for the on-chip Yagi-Uda antenna and shows the antenna matching well with a  $50 \Omega$  source impedance at 63 GHz.

#### B. Parameter Extraction

The material properties we extracted from our test chip measurements are: a) relative effective permittivity ( $\epsilon_r$ ) of the IC dielectric between metal layers, and b) loss tangent ( $\tan\delta$ ), a measure of loss of the IC dielectric.

Conductivity ( $\sigma$ ) of the metal layers and the lossy silicon (Si) substrate are also important properties that were extracted, but are not presented here. We used two methods taught by Kim [22] to extract  $\epsilon_r$  of the  $SiO_2$  (silicon dioxide) dielectric.

The first method uses a simple capacitor-type approach, however a drawback to this method is the inability to measure  $\tan\delta$ . The second method is more complicated and uses

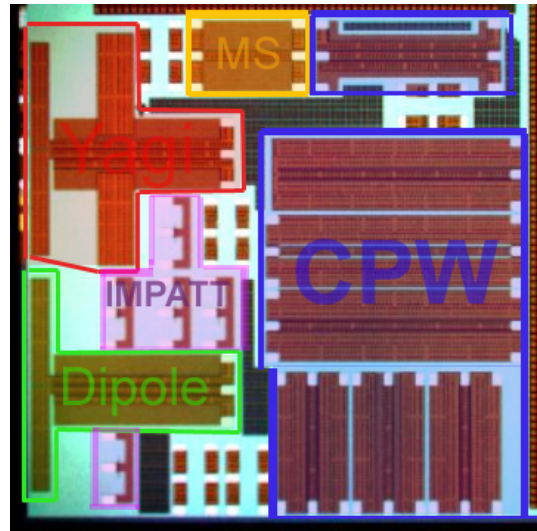


Fig. 3. Microscope image of a low cost 180 nm CMOS test chip used to create millimeter-wave on-chip antennas and RFICs. On-chip antennas can be phased in an array to create a highly directional beam for radar and communication.

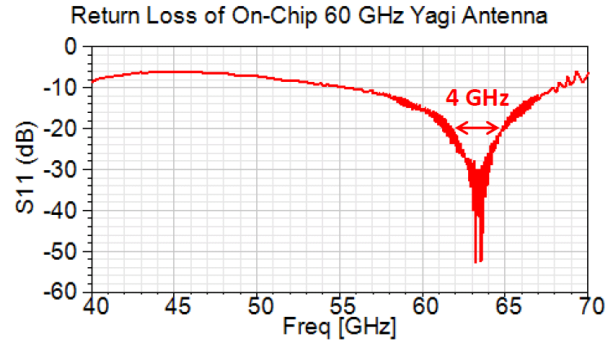


Fig. 4. Return loss ( $S_{11}$ ) of the on-chip 2-element Yagi antenna when measured with a Vector Network Analyzer (VNA) and  $50 \Omega$  source impedance. The on-chip antenna shows excellent matching at millimeter-wave frequencies, and a  $-20\text{dB } S_{11}$  bandwidth of 4 GHz.

transmission lines (T-Lines) to extract both  $\epsilon_r$  and  $\tan\delta$ .

The first method uses a capacitor approach by measuring the capacitance of a probe pad constructed on-chip. Figure 5 shows how probe pads can be modified into a parallel plate capacitor with a metal layer connecting the coplanar grounds as the bottom plate and the signal line as the top plate. In our chip, metal layer 1 (the bottom-most metal layer) was used to connect the coplanar grounds to form the capacitor.

Probe pads must be completely isolated as a stand-alone structure on the chip to measure  $S_{11}$  in both phase and magnitude. We use a simple series R-C circuit model to represent the probe pad as seen in Figure 5. To determine the values of  $R_{pad}$  and  $C_{pad}$ , we measure the  $S_{11}$  parameter and convert it into an input impedance,  $Z_{11}$ , using Equation 1, where  $Z_o$  is the source impedance of our measurement system ( $50 \Omega$ ). This is the S-Parameter to Z-Parameter transformation for a one-port microwave network [23]. For our simple model, the imaginary part of  $Z_{11}$  represents the series capacitor,  $C_{pad}$  (2). Since the area,  $A$ , of the probe pads is user-specified ( $40 \times 60 \mu\text{m}$  in our design) and the separation distance,  $d$

### IC Probe Pad Cross Section

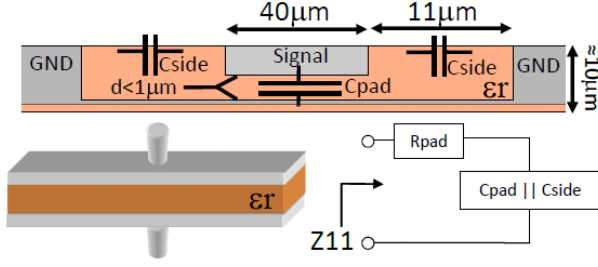


Fig. 5. A parallel plate capacitor approximation using probe pads to find the permittivity of the IC dielectric. A simple model assumes a small resistive loss,  $R_{pad}$ , in series with a large capacitor,  $C_{pad}$ . An enhanced model includes two small side capacitances,  $C_{side}$ , in parallel with  $C_{pad}$ .

(typically less than  $1\mu\text{m}$ ), is specified by the foundry, the  $\epsilon_r$  of the dielectric can be extracted using (3).

$$Z_{11} = Z_o \times \frac{1 + S_{11}}{1 - S_{11}}, \quad (1)$$

$$\text{Im}\{Z_{11}\} = \frac{1}{j\omega C}, \quad (2)$$

$$C = \frac{A\epsilon_o\epsilon_r}{d}. \quad (3)$$

We found  $\text{Im}\{Z_{11}\}$  from measurements over frequency and solved for  $C$  in (2). Then, given that  $A$ ,  $C$ ,  $d$ , and  $\epsilon_o$  are known, we found  $\epsilon_r$ . This parallel-plate capacitor model (3) yields a relative permittivity of about 4.32 at mmWave frequencies, as seen in Figure 8 (denoted “Probe Pad Epsilon (Simple)”). This approach does not take into account the side and fringing capacitance between the signal and coplanar grounds. The distance between the signal and coplanar grounds is  $11\mu\text{m}$  in our chip, which adds some additional capacitance parallel to  $C_{pad}$ . These additional capacitances add to overall capacitance and lower the extracted permittivity. In an enhanced model, we include the effects of the small side capacitance,  $C_{side}$ , between signal and ground. Using this enhanced model, the extracted  $\epsilon_r$  decreases to 4.22 as seen in Figure 8 (denoted as “Probe Pad Epsilon (Enhanced)”). As mentioned earlier, this probe pad capacitor method is unable to measure  $\tan\delta$ , the ratio of the imaginary part of  $\epsilon_r$ ,  $\epsilon''$ , to the real part,  $\epsilon'$ . A complex value of permittivity is needed to find loss tangent.

The second method for extracting permittivity uses transmission lines (T-Lines) since T-Line properties are only a function of cross-sectional geometry and dielectric permittivity. The properties of a T-Line can be represented by two complex numbers: the characteristic impedance ( $Z_o$ ), and the propagation constant ( $\gamma$ ).  $\gamma$  is composed of the real part,  $\alpha$ , which is the attenuation constant (loss per unit distance) and the imaginary part,  $\beta$ , which is the phase constant (radians per unit distance) as seen in Equation 4.

$$\gamma = \alpha + j\beta \quad (4)$$

By measuring  $Z_o$ , and  $\gamma$ , and by knowing the geometry of the transmission line, we can extract the complex  $\epsilon_r$  using analytical equations from T-Line handbooks [24]. Alternatively,

knowing  $\epsilon_r$  allows one to find  $Z_o$  and  $\gamma$ . For example, the  $Z_o$  of a Grounded CPW (GCPW) T-Line is given in [24] as:

$$Z_o = \frac{\eta_0}{2.0\sqrt{\epsilon_{eff}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k'_1)}}, \quad (5)$$

where  $k, k', K(k), K(k_1), \epsilon_{eff}$  are functions of physical spacings of the T-Line geometry (lengths, widths) and permittivity of the dielectric, respectively. By measuring  $Z_o$ , and knowing the physical dimensions of the T-Line (e.g. computing  $K(k)$ ), the relative permittivity can be extracted. Because this is a complex permittivity,  $\tan\delta$  can also be extracted.

The definition of loss tangent is (6)[23]. The term  $(\omega\epsilon'' + \sigma)$  can be considered the total effective conductivity. If we assume a good dielectric, then  $\sigma$  is near zero and can be disregarded, yielding:

$$\tan\delta = \frac{\omega\epsilon'' + \sigma}{\omega\epsilon'} \approx \frac{\epsilon''}{\epsilon'}. \quad (6)$$

GCPW T-Lines were chosen instead of microstrip due to their compatibility with the GSG probe tips. Additionally, GCPWs have metal shielding from the substrate to minimize loss. The difficulty of extracting  $Z_o$  and  $\gamma$ , especially for mmWave, is demonstrated by the many number of papers that have been written on accurately measuring S-parameters for T-Lines. Shih [25], recommends odd multiples of quarter wavelength T-lines for characterization to minimize “measurement uncertainties and junction discontinuities” as opposed to half-wavelength T-lines. T-Lines of roughly quarter-wavelength for mmWave frequencies were fabricated. The length of these T-Lines are  $l = 550\mu\text{m}$ . Probe pads ( $40 \times 60\mu\text{m}$ ) were added on each side of the T-Line as seen in the microscope image of Figure 6. The brown areas in Figure 6 are metal while the white square areas are probe pads for the GSG probes tips (in black). The probe pads

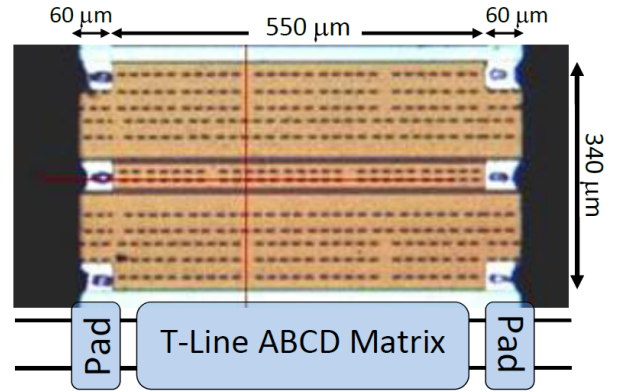


Fig. 6. Microscope image of the entire quarter-wavelength T-Line structure with probe pads. The T-Line-probe pad structure can be modeled as a cascade of ABCD matrices.

must be de-embedded to not taint the T-Line measurements. Transmission matrices (also known as “ABCD” matrices) are used to easily de-embed the probe pads from the T-Line. The ABCD matrix for the probe pad R-C model can be written as the product of (7) and (8) for the series resistance,  $R_{pad}$ , and the shunt capacitance,  $C_{pad}$ , [23].



$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{SeriesResistor} = \begin{pmatrix} 1 & R_{pad} \\ 0 & 1 \end{pmatrix} \quad (7)$$

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{ShuntCapacitor} = \begin{pmatrix} 1 & 0 \\ C_{pad} & 1 \end{pmatrix} \quad (8)$$

A cascaded block diagram of the ABCD matrices for probe pads and T-Line as seen in Figure 6 and mathematically in Figure 7 demonstrates how to de-embed the probe pads. The  $R_{pad}$  and  $C_{pad}$  S-parameter measurements from the probe pad capacitor method were used. Two port S-Parameter measurements were taken of the entire T-Line-probe pad structure and converted to an equivalent ABCD matrix [23]. The effects of the probe pads on the measured T-Line structure can be mathematically removed by matrix inversion as seen in the Figure 7 equation. This same process was used in [22].

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{Meas.} = \begin{pmatrix} 1 & R_{pad} \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 \\ C_{pad} & 1 \end{pmatrix} \cdot \begin{pmatrix} A & B \\ C & D \end{pmatrix}_{TLine} \cdot \begin{pmatrix} 1 & 0 \\ C_{pad} & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & R_{pad} \\ 0 & 1 \end{pmatrix}$$

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{TLine} = \begin{pmatrix} 1 & 0 \\ C_{pad} & 1 \end{pmatrix}^{-1} \cdot \begin{pmatrix} 1 & R_{pad} \\ 0 & 1 \end{pmatrix}^{-1} \cdot \begin{pmatrix} A & B \\ C & D \end{pmatrix}_{Meas.} \cdot \begin{pmatrix} 1 & R_{pad} \\ 0 & 1 \end{pmatrix}^{-1} \cdot \begin{pmatrix} 1 & 0 \\ C_{pad} & 1 \end{pmatrix}^{-1}$$

Fig. 7. The S-Parameters contains parasitic probe pad measurements embedded with the desired transmission line measurement. To de-embed the probe pads, convert S-parameters to ABCD parameters [23] and remove the cascaded pad structures with matrix inversion.

With the probe pads de-embedded,  $Z_o$  and  $\gamma$  of the transmission line can be calculated using (9) where  $l$  is the length of the T-Line (550  $\mu\text{m}$  in Figure 6) [23]. Measured parameter ‘‘A’’ in (9) can be used to extract  $\gamma$ .  $Z_o$  can then be extracted using  $\gamma$ ,  $l$ , and either parameter ‘‘B’’ or ‘‘C’’.

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{TLine} = \begin{pmatrix} \cosh(\gamma l) & Z_o \sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_o} & \cosh(\gamma l) \end{pmatrix} \quad (9)$$

The complex  $\epsilon_r$  of the dielectric can be calculated from  $Z_o$  using (5) [24]. The extracted  $\epsilon_r$  and  $\tan\delta$  across frequency are shown in Figure 8 and Figure 9, respectively. We see that the extracted relative permittivity,  $\epsilon_r$ , of the IC dielectric between the enhanced probe pad technique and the transmission line technique are in good agreement at mmWave frequencies. The extracted loss tangent is small and climbs linearly from 32 to 64 GHz.

Figure 10 shows a comparison of the T-Line  $Z_o$  between simulation and measurement. Ansoft’s Q3D extractor and HFSS were used to perform simulations using the extracted  $\epsilon_r$  value of 4.22 from the T-Line at mmWave frequencies. The  $Z_o$  matches well between simulation and measurement. The phase constant,  $\beta$  (from  $\gamma$ ), of the T-Line was also compared between simulation and measurement as seen in Figure 11.

Figure 11 confirms  $\beta$  is a linear function of frequency for a low loss T-Line [23]. For 60 GHz, the extracted  $\beta$  was about 2.5 radians per mm or a wavelength of 2.51 mm. Quarter wavelength T-Lines would have a length of 627.5  $\mu\text{m}$ .

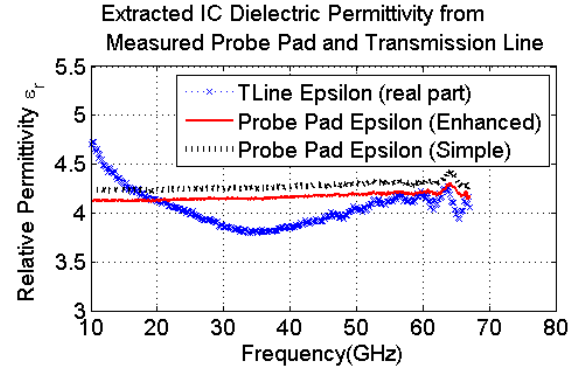


Fig. 8. Comparison of the predicted IC dielectric permittivity,  $\epsilon_r$ , from the measured transmission line versus the predicted value from the measured probe pad. The ‘‘simple’’ probe pad data assumes a simple parallel-plate capacitor model (Fig. 5). ‘‘Enhanced’’ probe pad model includes the small (yet significant) side capacitance from co-planar grounds.

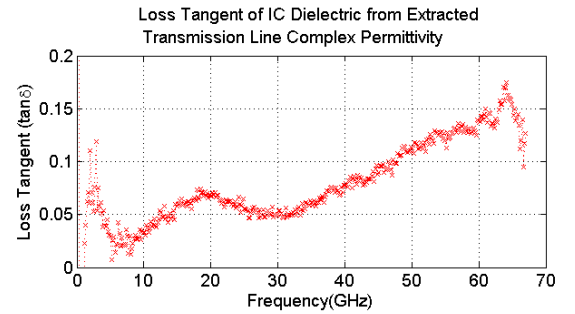


Fig. 9. The extracted IC dielectric loss tangent ( $\tan\delta$ ) from the measured transmission line relative permittivity,  $\epsilon_r$ , using (6).

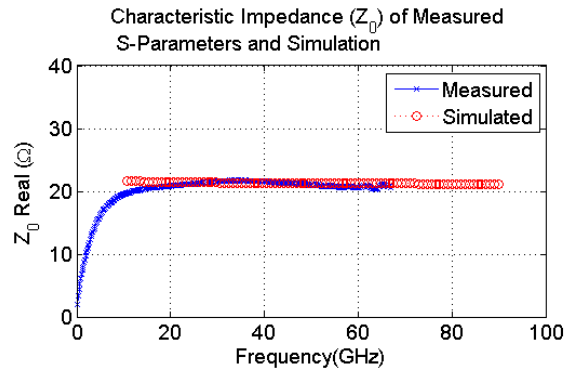


Fig. 10. Comparison between the measured characteristic impedance,  $Z_o$ , of the transmission line and the simulation results using the transmission line estimated dielectric permittivity,  $\epsilon_r$ , of 4.22 at 60 GHz.

## V. SUMMARY

As frequencies increase and wavelengths shrink, complete RF systems with antennas can be fabricated on silicon. We

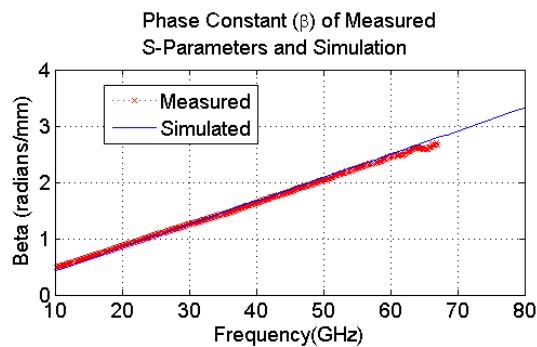


Fig. 11. Comparison between the measured phase constant,  $\beta$ , of the transmission line and the simulation results using the transmission line estimated dielectric permittivity,  $\epsilon_r$ , of 4.22 at 60 GHz.

demonstrated key techniques for extracting electromagnetic properties of RF integrated circuits for accurate design. We showed how test capacitors and transmission lines provide useful parameters such as relative permittivity of the IC dielectric. This paper provides a vision of creating low-cost, high-gain antennas in older CMOS processes for massive markets where reducing costs of a few cents per chip will amount to large savings. Older and mature CMOS technology can be used to provide benefits for millimeter-wave and RF electronic devices. Understanding the electrical behavior of the IC materials in millimeter-wave and terahertz frequencies is crucial for successful deployment and commercialization, yet these may be unknown by the foundry.

## VI. ACKNOWLEDGMENT

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