A Mathematical Framework to Design Transcription Based Boolean Gates

Weekly Research Report #2

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1 Introduction

In this report, we will consider a simple design schema for simple boolean circuits that are based on transcriptional regulatory networks.

The major building-block of our circuits will be the simple single-input-single-output model we considered in the previous model. In this simple model, if we took X concentration as the input and Y as the output then the average behaviour is modeled by:

$$Y \quad = \quad f(X) = \frac{\beta}{1 + \left(\frac{X}{K}\right)^n}$$

Note that, this model is a over-simplified representation of all protein-DNA interactions, transcription and translation processes. Two major points that model ignores are the leakage in the transcription and the fluctuations originated from the discrete nature of the processes (inherent noise). Here we *assumed* the leakage is small compared to the K parameters and we are operating at X levels that are not close to K so both of the effects are ignored but this assumptions requires more justification.

2 Nomenclature

For the rest of the report, our simple equation above is represented by $X \longrightarrow_j^i Y$ where i is the index for the simple devices and j is the copy number of the relevant gene:

$$Y \quad = \quad f_i(X) = \frac{j\beta_i}{1 + \left(\frac{X}{K_i}\right)^{n_i}}.$$

Additionally, input and output protein concentrations are represented by $I_1, \ldots, I_n$ and $O_1, \ldots, O_m$, respectively.

3 Simple Boolean Gates

3.a Buffer and Inverter

Our simple device is simply stands for a buffer or inverter:

$$I \longrightarrow_j^i O$$

where its qualitative behavior depends on the sign of n_i:

- Buffer: $n_i < 0$
- Inverter: $n_i > 0$

3.b AND/OR/NAND/NOR Gates

For the sake of simplicity for the design we will consider only a simple structure that can implement all of the four the of the gates under certain conditions.

The structure is:

$$I_1 \longrightarrow_{j_1}^1 X, \qquad I_2 \longrightarrow_{j_2}^2 X, \qquad X \longrightarrow_{j_3}^3 O,$$

also we will impose extra restrictions on the parameters to get the desired behavior:

$$0 < K_3 < j_1\beta_1, \qquad 0 < K_3 < j_2\beta_2,$$

and the behaviour can be summarized as:

- OR : $n_1 < 0, \quad n_2 < 0, \quad n3 < 0$
- AND: $n_1 > 0, \quad n_2 > 0, \quad n3 > 0$
- NOR: $n_1 < 0, \quad n_2 < 0, \quad n3 > 0$
- NAND: $n_1 > 0, \quad n_2 > 0, \quad n3 < 0$

3.b.1 An Alternative Implementation

For the same structure if we modify the restrictions into:

$$K_3 > j_1\beta_1, \qquad K_3 > j_2\beta_2, \qquad K_3 < j_1\beta_1 + j_2\beta_2,$$

then the behavior of the device can also be modified as:

- OR : $n_1 > 0, \quad n_2 > 0, \quad n3 > 0$
- AND: $n_1 < 0, \quad n_2 < 0, \quad n3 < 0$
- NOR: $n_1 > 0, \quad n_2 > 0, \quad n3 < 0$
- NAND: $n_1 < 0, \quad n_2 < 0, \quad n3 > 0$

4 Connection of Simple Devices

4.a Signal Matching

In this section, we will study the necessary conditions to connect two devices without loosing functionality. In the literature this problem is known as *signal matching*.

In our model, the signal levels at the outputs of the devices is characterized by β and j parameters and input levels are characterized by K's. To keep the design procedures simple, we will use the simplest relation to assure the compatibility; to make $I \longrightarrow^{1}_{j_1} X$ and $X \longrightarrow^{2}_{j_2} O$ compatible we require $0 < K_2 < j_1\beta_1$.

As an analogy to the electrical circuitry: our structures stand for electrical components and our conditions on K and β's are the cables connecting them each other.

4.b Simplification

The simplification for a given circuit can be considered on two different levels. The first one is at the functional level which is simply the classical boolean methods used in digital design such as Karnough maps, etc. Since those methods are well studied we will assume that our functional description already optimized in this sense and contains the minimum number of gates.

The second level of simplification is in terms of the number of genetic parts and some techniques for such optimization are also studied and borrowed from code optimization techniques.

However note that, in our framework after connecting simple gates to produce the circuitry only replacing the cascade buffers/inverters with only one buffer/inverter would be enough to simplify the circuit effectively. This idea is demonstrated below for a small circuit.

4.b.1 Example: $O = AND(NOT(I_1), I_2)$

- NOT gate:

$$I_1 \longrightarrow^{1}_{j_1} X, \qquad n_1 > 0$$

- AND gate:

$$X \longrightarrow^{2}_{j_2} Y, \qquad I_2 \longrightarrow^{3}_{j_3} Y, \qquad Y \longrightarrow^{4}_{j_4} O$$
$$n_2 > 0, \qquad n_3 > 0, \qquad n_4 > 0,$$
$$0 < K_4 < j_2\beta_2, \qquad 0 < K_4 < j_3\beta_3$$

- Connection:

$$0 < K_2 < j_1\beta_1$$

- Simplified circuit:

$$I_1 \longrightarrow^{1}_{j_1} Y, \qquad I_2 \longrightarrow^{2}_{j_2} Y, \qquad Y \longrightarrow^{3}_{j_3} O$$
$$n_1 < 0, \qquad n_2 > 0, \qquad n_3 > 0$$
$$0 < K_3 < j_1\beta_1, \qquad 0 < K_3 < j_2\beta_2$$

- Note that, in this example I_1 and I_2 are inputs from outside and their characteristics did not considered. In other words, we assumed K_1 and K_2 are appropriately chosen to sense I_1 and I_2 levels effectively.

5 To-do List for Next Week(s)

5.a Anil

5.a.1 Reliability

- In what sense, against what kind of failures?
- Exactly which tools?
- ...

5.a.2 Complex Devices

- Under the assumption of a working clock ?
- Time scales ?
- ...

5.b Felix

5.b.1 Application Details

- Details and other physical challenges
- Laboratory techniques and procedures
- Literature
- ...