CS202 (003): Operating Systems I/O

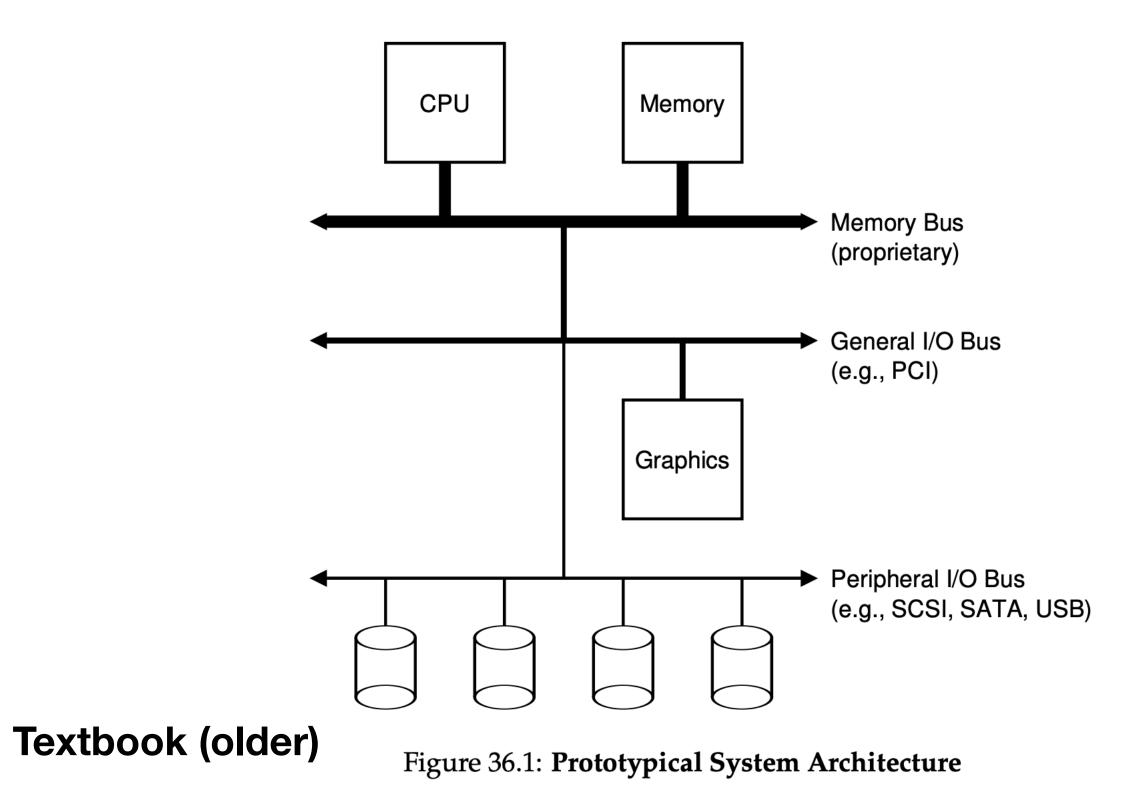
Instructor: Jocelyn Chen

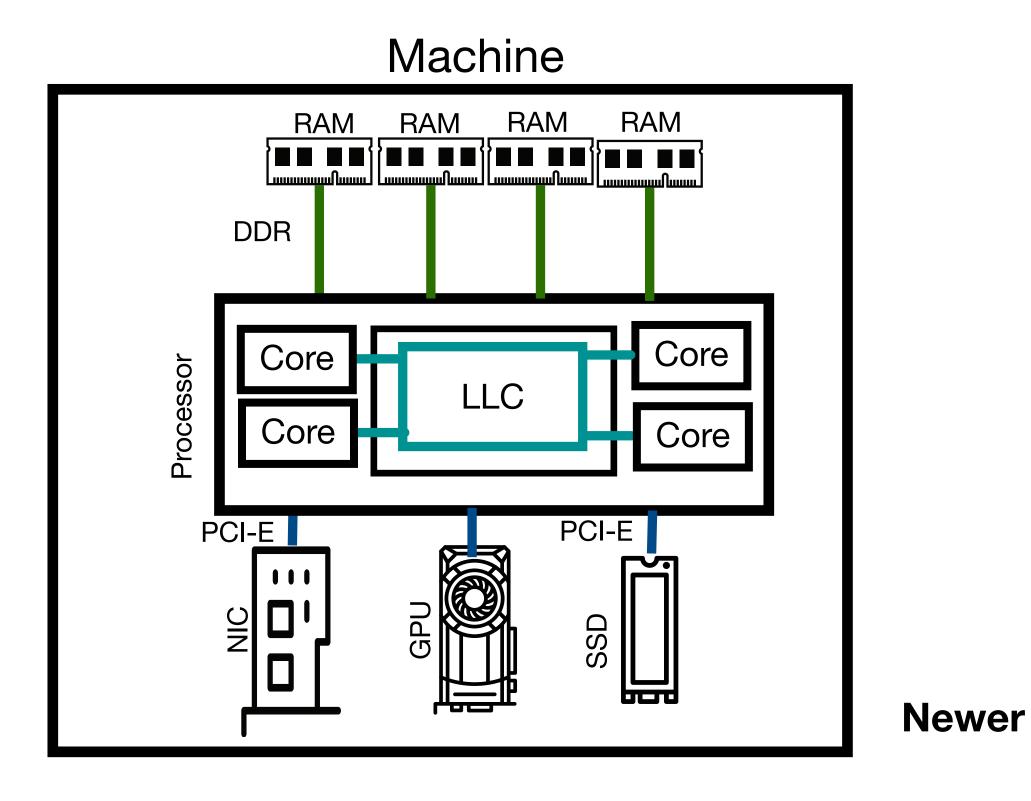
Most of the materials covered in this slide come from the lecture notes of Mike Walfish's CS202



Last Time

I/O Architecture at a high-level





Mechanics of Communication

Explicit I/O instructions

outb, inb, outw, inw

WeesyOS boot.c (handout)

Control Register: Address 0x3F6 = 0x08 (0000 1RE0): R=reset, E=0 means "enable interrupt" each register stores 8-bit data Command Block Registers: Address 0x1F0 = Data PortAddress 0x1F1 = ErrorAddress 0x1F2 = Sector CountAddress 0x1F3 = LBA low byte Address 0x1F4 = LBA mid byte Address 0x1F5 = LBA hi byte Address 0x1F6 = 1B1D TOP4LBA: B=LBA, D=drive Address 0x1F7 = Command/statusStatus Register (Address 0x1F7): 4 2 7 3 0 1 CORR IDDEX ERROR BUSY READY FAULT SEEK DRQ Error Register (Address 0x1F1): (check when ERROR==1) 5 4 3 7 6 0 MCR ABRT TONF AMNF BBK UNC MC IDNF = Bad Block BBK = Uncorrectable data error UNC = Media Changed MC IDNF = ID mark Not Found = Media Change Requested MCR ABRT = Command aborted TONF = Track 0 Not FoundAMNF = Address Mark Not Found

Figure 36.5: The IDE Interface

LBA: Linear block address (28-bit in the handout) describes storage locations each sector gets a unique number starting from 0

Status is read-only Command is used to add instructions to the disk

(Integrated Device Electronics): connection between a bus on the motherboard and disk storage

https://www.rfcandy.biz/communication/ide.html



```
static int ide_wait_ready() {
  while (((int r = inb(0x1f7)) \& IDE_BSY) || !(r \& IDE_DRDY))
    ; // loop until drive isn't busy
  // return -1 on error, or 0 otherwise
static void ide_start_request(struct buf *b) {
  ide_wait_ready();
  outb(0x3f6, 0);
                                  // generate interrupt
                                  // how many sectors?
  outb(0x1f2, 1);
  outb(0x1f3, b->sector & 0xff); // LBA goes here ...
  outb(0x1f4, (b->sector >> 8) & 0xff; // ... and here
  outb(0x1f5, (b->sector >> 16) & 0xff); // ... and here!
  outb(0x1f6, 0xe0 | ((b->dev&1)<<4) | ((b->sector>>24)&0x0f));
  if(b->flags & B_DIRTY) {
    outb(0x1f7, IDE_CMD_WRITE);
                                  // this is a WRITE
    outsl(0x1f0, b->data, 512/4); // transfer data too!
  } else {
    outb(0x1f7, IDE_CMD_READ);
                                  // this is a READ (no data)
                                     handle read/write request
void ide_rw(struct buf *b) {
 acquire(&ide_lock);
  for (struct buf **pp = &ide_queue; *pp; pp=&(*pp)->qnext)
                                   // walk queue
   ;
                                   // add request to end
  *pp = b;
                                  // if q is empty
  if (ide_queue == b)
                                  // send req to disk
   ide_start_request(b);
  while ((b->flags & (B_VALID|B_DIRTY)) != B_VALID)
    sleep(b, &ide_lock);
                                   // wait for completion
  release(&ide_lock);
void ide_intr() { handle disk interrupt when operation complete
  struct buf *b;
  acquire(&ide_lock);
  if (!(b->flags & B_DIRTY) && ide_wait_ready() >= 0)
   insl(0x1f0, b->data, 512/4); // if READ: get data
  b->flags |= B_VALID;
  b->flags &= ~B_DIRTY;
                                   // wake waiting process
  wakeup(b);
  if ((ide_queue = b->qnext) != 0) // start next request
    ide_start_request(ide_queue); // (if one exists)
  release(&ide_lock);
```

Figure 36.6: The xv6 IDE Disk Driver (Simplified)

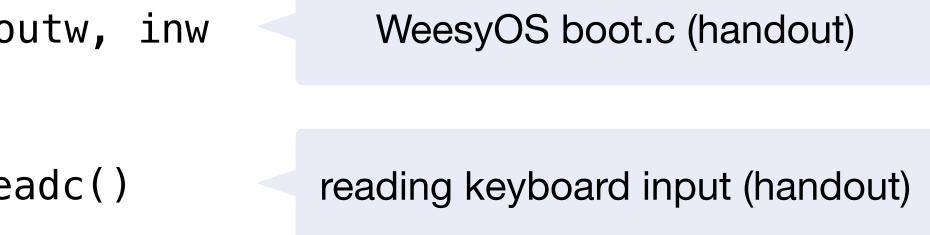
read: data is read and valid bit is set write: data is written and dirty bit is cleaned

Explicit I/O instructions

outb, inb, outw, inw

keyboard_readc()

Mechanics of Communication

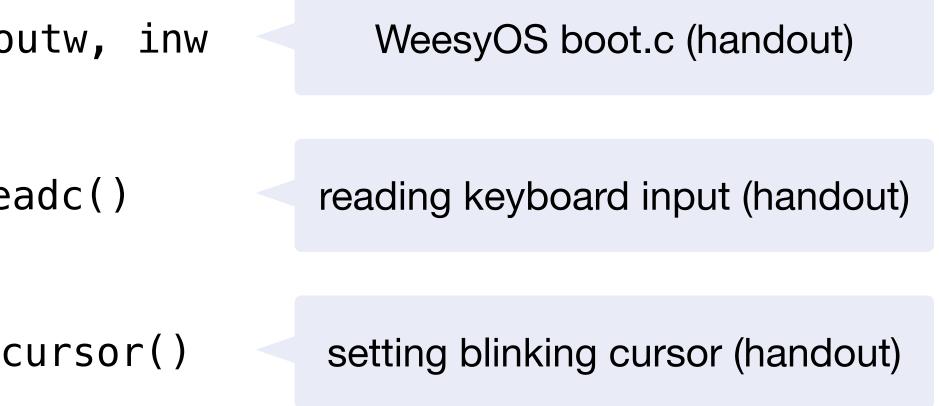


Explicit I/O instructions outb, inb, outw, inw

keyboard_readc()

console_show_cursor()

Mechanics of Communication

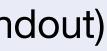


Mechanics of Communication

Most of the physical address space contains regular RAM However, the lower memory addresses (650K-1MB) are special - they don't refer to actual RAM

Memory-mapped I/O

WeesyOS console printing (handout)



Mechanics of Communication

Explicit I/O instructions

Memory-mapped I/O

Interrupts

Mechanics of Communication

Explicit I/O instructions

Memory-mapped I/O

Interrupts

Through memory

Both CPU and the device see the same memory, so they can use shared memory to communicate. (eg. DMA)

Polling vs. Interrupt (vs. busy waiting)

Busy Waiting

while (!device_is_ready()) {
 // CPU is stuck here,
 repeatedly checking
 // Consuming CPU cycles doing
 nothing useful
}

Simple but inefficient CPU stuck here running at full speed

Polling vs. Interrupt (vs. busy waiting)

Busy Waiting

while (!device_is_ready()) {
 // CPU is stuck here,
 repeatedly checking
 // Consuming CPU cycles doing
 nothing useful
}

Polling

```
void poll_device() {
  while (1) {
    if (device_is_ready())
      { process_device_data(); }
    // Sleep/delay for a set
    interval
    sleep_ms(100); // Check every
    100ms
  }
}
```

System checks device status at regular intervals Lower CPU usage



Polling vs. Interrupt (vs. busy waiting)

Busy Waiting

while (!device_is_ready()) { // CPU is stuck here, repeatedly checking // Consuming CPU cycles doing nothing useful

set_interrupt_handler

do_other_work();

it triggers interrupt

Most sophisticated approach If interrupt rate is high, we can get **livelock**

Interrupts

Polling

```
// CPU sets up interrupt handler
   (device_interrupt_handler);
```

```
// CPU goes on to do other useful work
```

```
// When device needs attention,
// and the handler runs automatically
void device_interrupt_handler() {
  // Handle the device's needs
  process_device_data();
```

```
void poll_device() {
  while (1) {
     if (device_is_ready())
         { process_device_data(); }
       // Sleep/delay for a set
```

```
interval
sleep_ms(100); // Check every
100ms
```



Programmed I/O vs. DMA (Direct memory access)

Programmed I/O

CPU writes data directly to device, and reads data directly from device.

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Programmed I/O

CPU writes data directly to device, and reads data directly from device.

DMA

CPU places some buffers in main memory.

Tells device where the buffers are Then "pokes" the device by writing to register Then device uses DMA to read or write the The CPU can poll to see if the DMA completed (or the device can interrupt the CPU when done).

CPU don't have to constantly deal with small amount of data transfer, the device can write the contents straight into memory

Software architecture: device drivers

Device drivers act as a bridge between hardware devices and the operating system kernel

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reset(): Initializes or resets the device ioctl(): Provides device-specific controls read()/write(): Standard data transfer operations handle_interrupt(): Manages hardware interrupts

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Device drivers act as a bridge between hardware devices and the operating system kernel

reset(): Initializes or resets the device ioctl(): Provides device-specific controls read()/write(): Standard data transfer operations handle_interrupt(): Manages hardware interrupts

Advantages: don't have to worry about the specific hardware implementation

- 1. Device drivers is per-OS and per-device (hard part cannot be reused)
- 2. Bugs in device drivers often bring down the entire machine

Example interface

ssues:

Synchronous vs. Asynchronous I/O

Synchronous I/O

When a process makes a system call (like read() or write()), it blocks (suspends) until the operation completes

The process enters a sleep state and cannot execute other codes

Control returns to process after operation finishes

Code is often more readable, but it is slow

Synchronous vs. Asynchronous I/O

Synchronous I/O

When a process makes a system call (like read() or write()), it blocks (suspends) until the operation completes

The process enters a sleep state and cannot execute other codes

Control returns to process after operation finishes

Async I/O

System calls return immediately, even if the operation isn't completed

Instead of blocking, the call returns a status indicating what would have happened

Check through polling or interrupt

Need to use platform-specific extensions to POSIX to do async I/O for files



Enjoy the spring break! (no class next week)