

# Ogre et Pythia: An invariance proof method for weak consistency models

Jade Alglave (MSR-Cambridge, UCL, UK)

Patrick Cousot (NYU, Emer. ENS, PSL)

POPL 2017

18 January 2017

# Objective

# Example (Peterson)

```
0: { w F1 false; w F2 false; w T 0; }
1: w[] F1 true
2: w[] T 2
3: do
5:   r[] R1 F2
6:   r[] R2 T
7: while R1  $\wedge$  R2  $\neq$  1
8:  $\neg$ at 28
9: w[] F1 false
10:
21:w[] F2 true;
22:w[] T 1;
23:do
25:   r[] R3 F1;
26:   r[] R4 T;
27:while R3  $\wedge$  R4  $\neq$  2;
28: $\neg$ at 8
29:w[] F2 false;
39:
```

critical section

# An invariance proof method for WCMs

- Extend Lamport's invariance proof method for parallel programs from **sequentially consistent** to **weak consistency models** so that
  - The **weak consistency model** is a *parameter* of the **proof**
  - We don't **have to redo the whole proof when changing the consistency model**

Note: Owicki & Gries is Lamport with auxiliary variables instead of programs counters

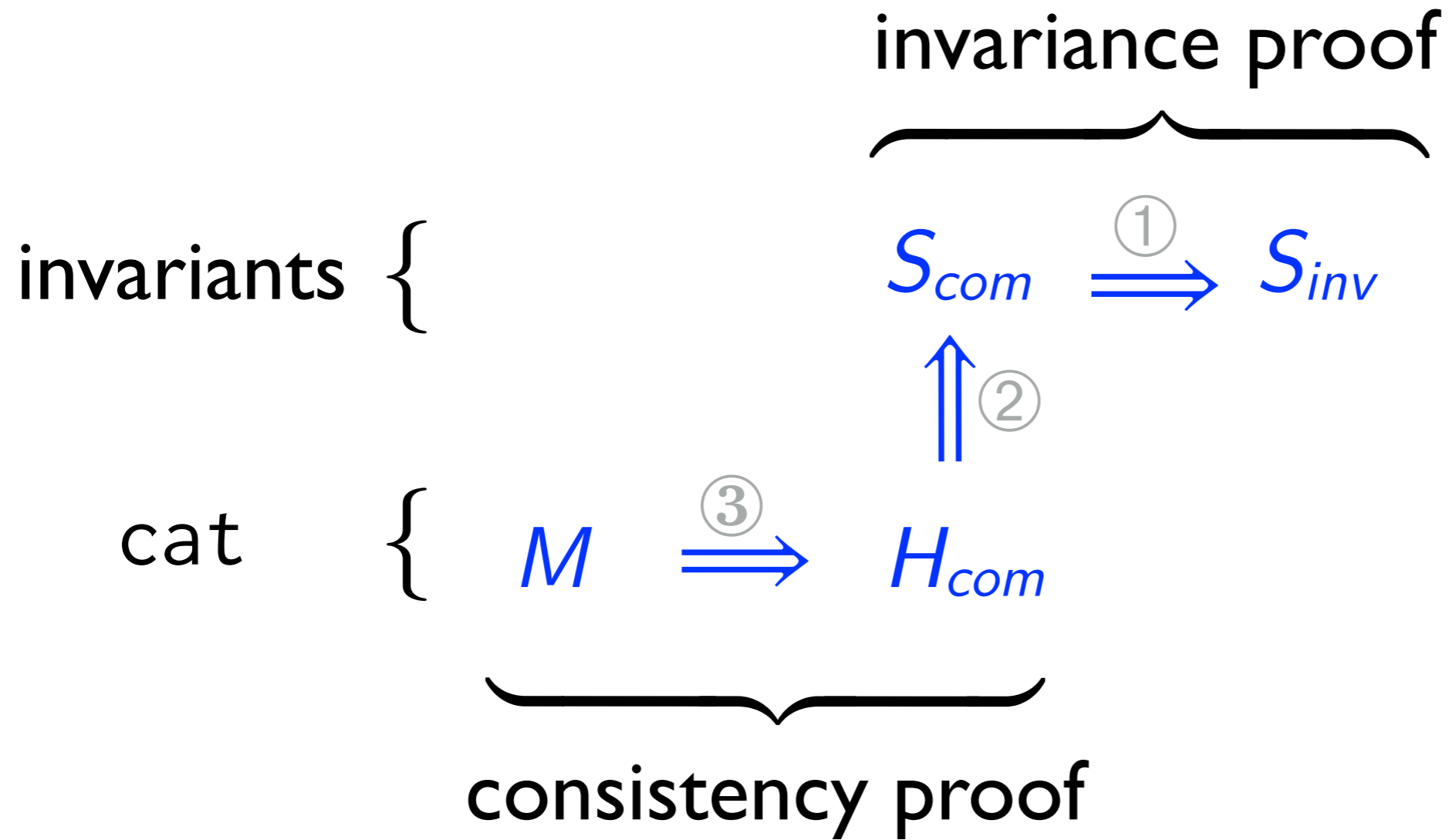
# Separating invariance from WCM

- The **invariance proof** (that a specification  $S_{inv}$  is invariant for a program):
  - Done for a **program consistency hypothesis**  $S_{com}$ :
    - Sufficient for the program to be correct
    - Or better, also necessary for correctness (weakest consistency model)
  - This program consistency hypothesis  $S_{com}$  is expressed as an invariant
  - sound and (relatively) complete

# Separating invariance from WCM

- Consistency proof:
  - a. The program consistency hypothesis  $S_{com}$  is strengthened into  $H_{com}$  written in a consistency specification language (e.g. cat)
  - b. A cat **architecture consistency model**  $M$  is shown to imply the cat program consistency model  $H_{com}$
- only b. to be redone when changing the architecture
- sound but possibly incomplete

# Methodology



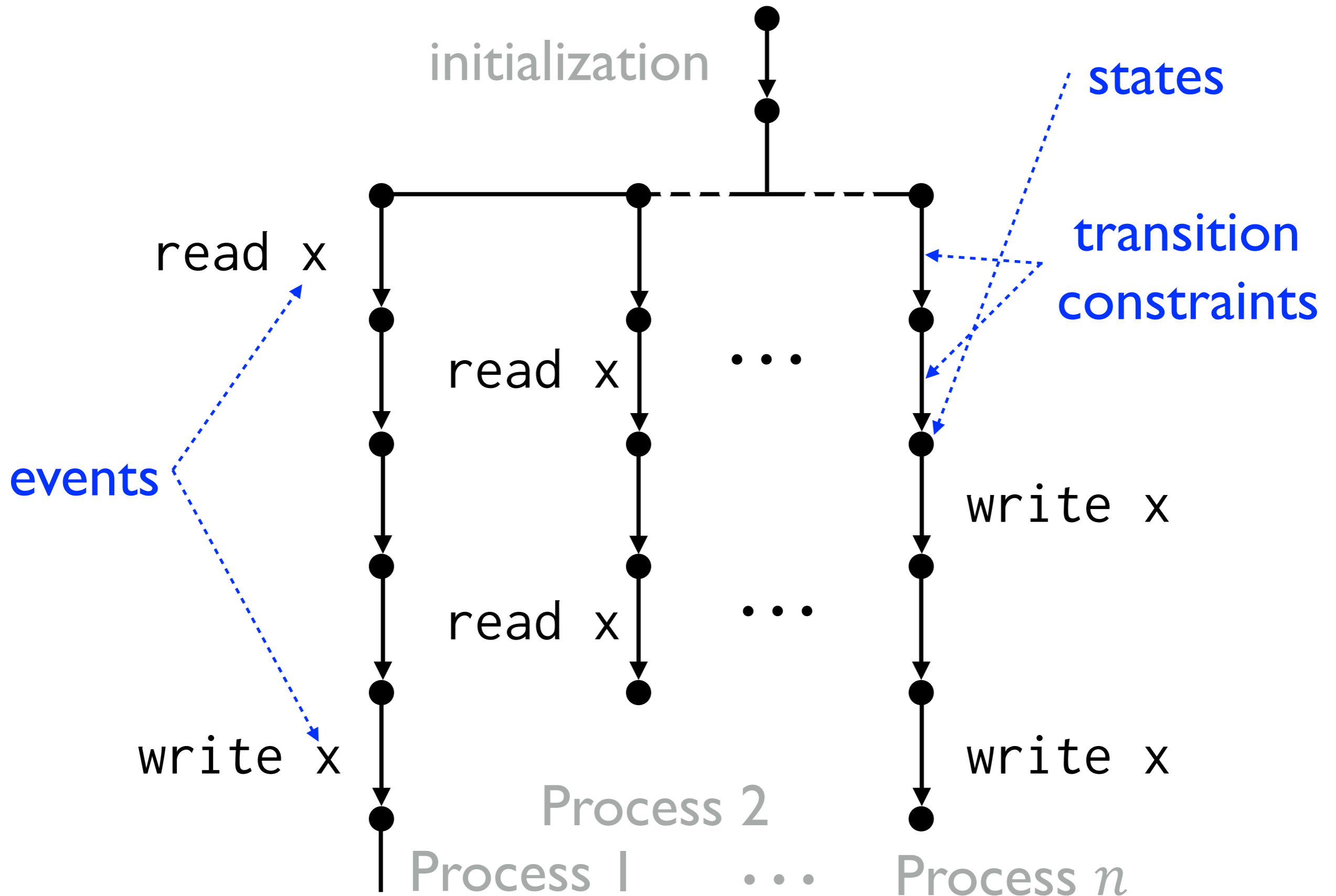
The invariance proof  
method is designed by  
abstract interpretation of  
an *analytic* semantics



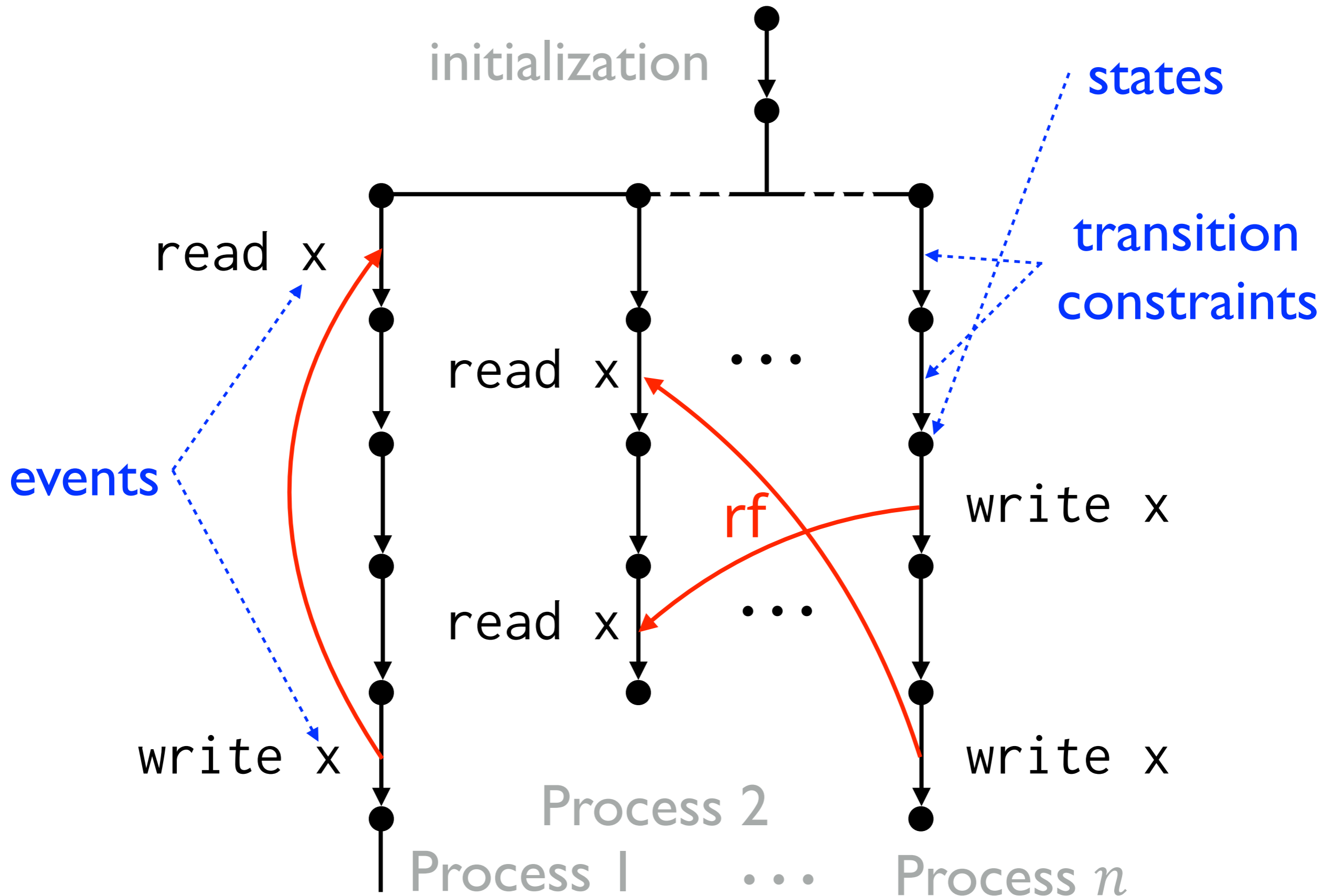
Analytic semantics  
=  
Anarchic semantics  
┌  
Weak consistency model

# The anarchic semantics

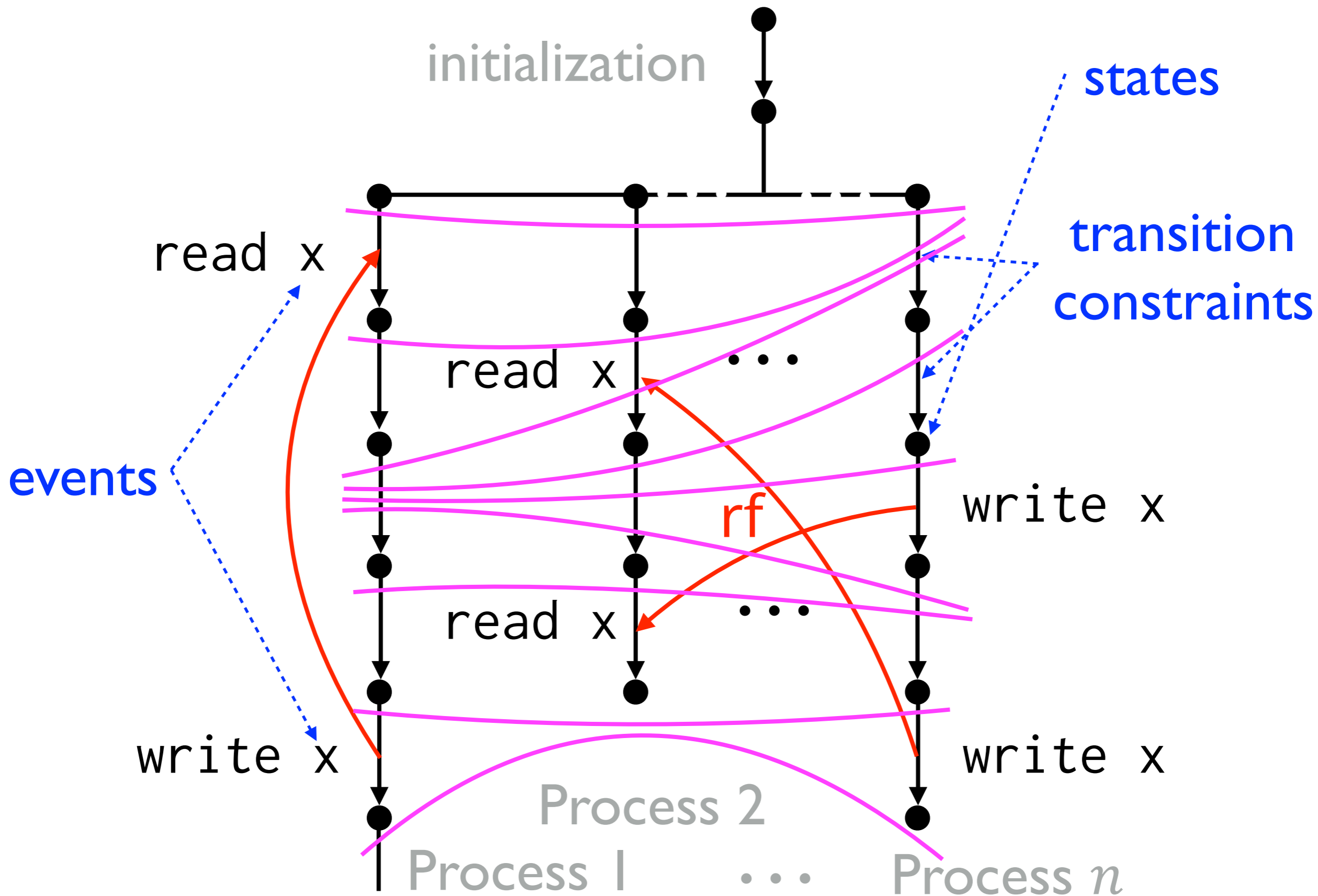
# The anarchic semantics



# The read-from relation $rf$



# Cuts



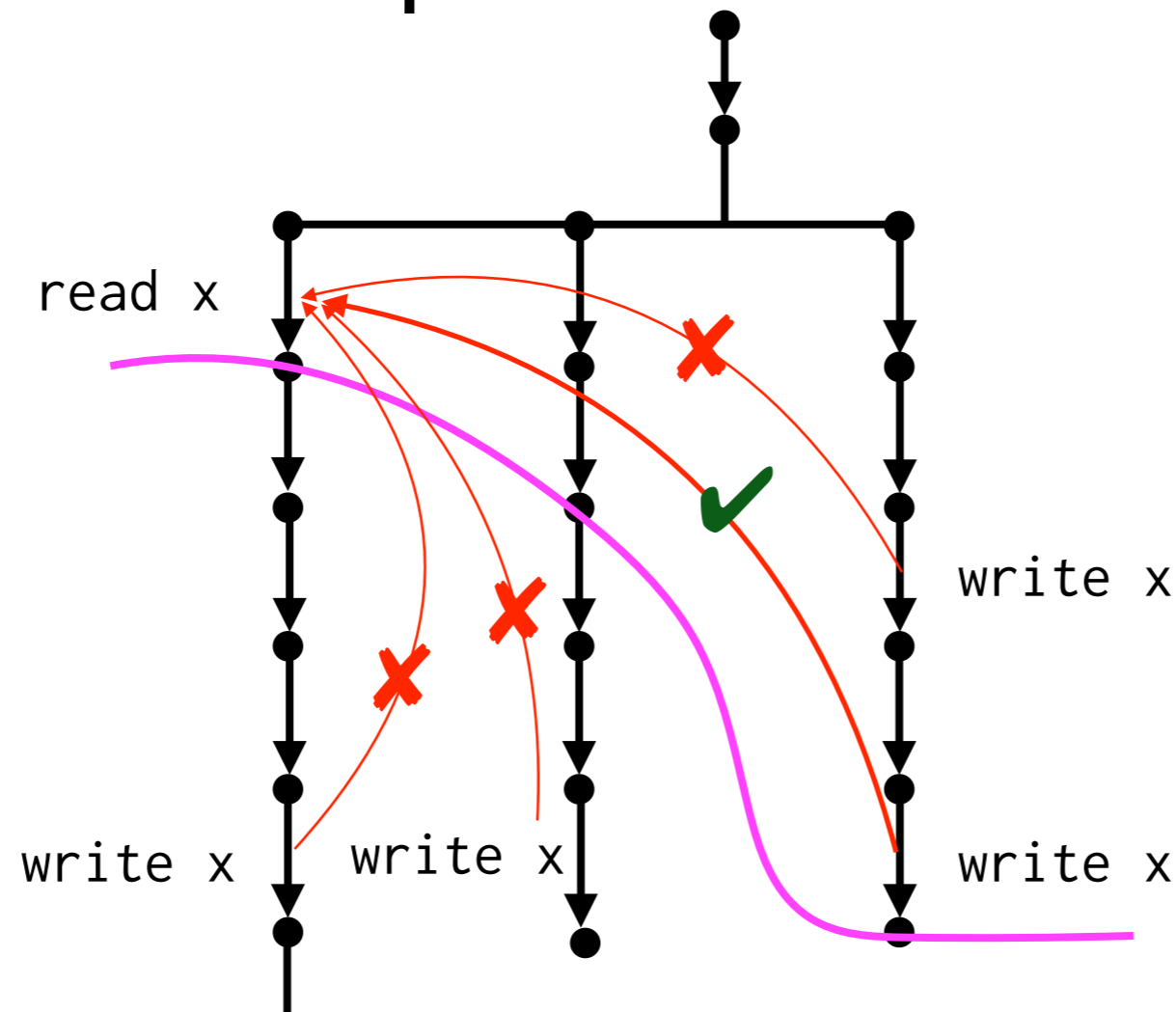
# Anarchic semantics of fences

- The anarchic semantics of (localized) fences is *skip* (the state is unmodified)
- Fences are *static marker events* used by the WCM in *cat* to restrict the read-from relation *rf*

# The weak consistency model

# Weak consistency models

- Put restrictions on the read-from relation  $rf$
- e.g. **sequential consistency**: a read at a cut reads from that last write in a process before that cut





# Difficulties

# Naming entities

- Invariants are **logical formulæ**
- can only describe entities that they **name**
- L/O-G use the **name** of shared variables to designate their current **value** in invariants

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- can only describe entities that they **name**
- L/O-G use the **name** of shared variables to designate their current **value** in invariants

## Difficulty

- Meaningless with WCMs since there is no notion of “the current value of a shared variable”

# What is known on communications?

- Each process only knows the value of the shared variables from its last read
- Need to be named → Pythia Variables

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- Each process only knows the value of the shared variables from its last read
- Need to be named → Pythia Variables

## Difficulty

- Its **dynamic**, not static!
- A program read action can read from a different write each time it is executed → **Stamps** (abstraction of local time)

# Back to the anarchic semantics

# State

- Per process:
  - A **stamp** (local time, no global time)
  - A **program counter**
  - The **value of the local variables** (registers) of the process
  - The stamped **pythia variables** (uniquely identifying all reads along a trace)
  - The **value of the pythia variables** (what was read)
- The read-from relation (**rf**)

# Example (Peterson)

```
0: { w F1 false; w F2 false; w T 0; }
```

```
P0:
```

```
1: w[] F1 true
```

```
2: w[] T 2
```

```
3: do {i}
```

```
4:   r[] R1 F2 { $\rightsquigarrow$  F24i}
```

```
5:   r[] R2 T { $\rightsquigarrow$  T5i}
```

```
6: while R1  $\wedge$  R2  $\neq$  1 {iend}
```

```
7: skip (* CS1 *)
```

```
8: w[] F1 false
```

```
P1:
```

```
10: w[] F2 true;
```

```
11: w[] T 1;
```

```
12: do {j}
```

```
13:   r[] R3 F1; { $\rightsquigarrow$  F113j}
```

```
14:   r[] R4 T; { $\rightsquigarrow$  T14j}
```

```
15: while R3  $\wedge$  R4  $\neq$  2; {jend}
```

```
16: skip (* CS2 *)
```

```
17: w[] F2 false;
```

Stamps (loop counters)

Stamps (on loop exit)



# Example (Peterson)

```
0: { w F1 false; w F2 false; w T 0; }
```

P0:

```
1: w[] F1 true
```

```
2: w[] T 2
```

```
3: do {i}
```

```
4:   r[] R1 F2 { $\rightsquigarrow$   $F2_4^i$ }
```

```
5:   r[] R2 T { $\rightsquigarrow$   $T_5^i$ }
```

```
6: while R1  $\wedge$  R2  $\neq$  1 {i_end}
```

```
7: skip (* CS1 *)
```

```
8: w[] F1 false
```

P1:

```
10: w[] F2 true;
```

```
11: w[] T 1;
```

```
12: do {j}
```

```
13:   r[] R3 F1; { $\rightsquigarrow$   $F1_{13}^j$ }
```

```
14:   r[] R4 T; { $\rightsquigarrow$   $T_{14}^j$ }
```

```
15: while R3  $\wedge$  R4  $\neq$  2; {j_end}
```

```
16: skip (* CS2 *)
```

```
17: w[] F2 false;
```

Stamps (loop counters)

Stamps (on loop exit)

Pythia variables

# The abstraction

# The invariance abstraction

- For each **process**

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- For each **process**
- For each **program point** of that process

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  - For each **execution** of the program

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- For each **execution** of the program
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**collect:**

- The **states of all processes**, and



# The invariance abstraction

- For each **process**
- For each **program point** of that process
- For each **execution** of the program
  - For each **cut** of that execution going through the program point of that process

**collect:**

- The **states of all processes**, and
- The **read-from relation** **rf**

# Example: Peterson

```

0: { w F1 false; w F2 false; w T 0; }
   {F1=false ∧ F2=false ∧ T=0} }
1: {R1=0 ∧ R2=0}
   w[] F1 true
2: {R1=0 ∧ R2=0}
   w[] T 2
3: {R1=0 ∧ R2=0}
   do {i}
4: {(i=0 ∧ R1=0 ∧ R2=0) ∨
   (i>0 ∧ R1=F24i-1 ∧ R2=T5i-1)}
   r[] R1 F2 {↗ F24i}
5: {R1=F24i ∧ (i=0 ∧ R2=0) ∨
   (i>0 ∧ R2=T5i-1)}
   r[] R2 T {↗ T5i}
6: {R1=F24i ∧ R2=T5i}
   while R1 ∧ R2≠1 {iend}
7: {¬F24iend ∨ T5iend=1}
   skip (* CS1 *)
8: {¬F24iend ∨ T5iend=1}
   w[] F1 false
9: {¬F24iend ∨ T5iend=1}

```

```

10: {R3=0 ∧ R4=0}
    w[] F2 true;
11: {R3=0 ∧ R4=0}
    w[] T 1;
12: {R3=0 ∧ R4=0}
    do {j}
13: {(j=0 ∧ R3=0 ∧ R4=0) ∨
    (j>0 ∧ R3=F113j-1 ∧ R4=T14j-1)}
    r[] R3 F1 {↗ F113j};
14: {R3=F113j ∧ (j=0 ∧ R4=0) ∨
    (j>0 ∧ R4=T14j-1)}
    r[] R4 T; {↗ T14j}
15: {R3=F113j ∧ R4=T14j}
    while R3 ∧ R4≠2 {jend};
16: {¬F113jend ∨ T14jend=2}
    skip (* CS2 *)
17: {¬F113jend ∨ T14jend=2}
    w[] F2 false;
18: {¬F113jend ∨ T14jend=2}

```

# Example: Peterson

0: { w F1 false; w F2 false; w T 0; }

{F1=false  $\wedge$  F2=false  $\wedge$  T=0} }

1: {R1=0  $\wedge$  R2=0}

w[] F1 true

2: {R1=0  $\wedge$  R2=0}

w[] T 2

3:

4:

4: { (i=0  $\wedge$  R1=0  $\wedge$  R2=0)  $\vee$   
 (i>0  $\wedge$  R1=F2<sub>4</sub><sup>i-1</sup>  $\wedge$  R2=T<sub>5</sub><sup>i-1</sup>) }

5: {R1=F2<sub>4</sub><sup>i</sup>  $\wedge$  (i=0  $\wedge$  R2=0)  $\vee$   
 (i>0  $\wedge$  R2=T<sub>5</sub><sup>i-1</sup>) }

r[] R2 T { $\rightsquigarrow$  T<sub>5</sub><sup>i</sup>}

6: {R1=F2<sub>4</sub><sup>i</sup>  $\wedge$  R2=T<sub>5</sub><sup>i</sup>}

while R1  $\wedge$  R2 $\neq$ 1 {i<sub>end</sub>}

7: { $\neg$ F2<sub>4</sub><sup>i<sub>end</sub></sup>  $\vee$  T<sub>5</sub><sup>i<sub>end</sub></sup>=1}

skip (\* CS1 \*)

8: { $\neg$ F2<sub>4</sub><sup>i<sub>end</sub></sup>  $\vee$  T<sub>5</sub><sup>i<sub>end</sub></sup>=1}

w[] F1 false

9: { $\neg$ F2<sub>4</sub><sup>i<sub>end</sub></sup>  $\vee$  T<sub>5</sub><sup>i<sub>end</sub></sup>=1}

10: {R3=0  $\wedge$  R4=0}

w[] F2 true;

11: {R3=0  $\wedge$  R4=0}

w[] T 1;

14: {R3=F1<sub>13</sub><sup>j</sup>  $\wedge$  (j=0  $\wedge$  R4=0)  $\vee$   
 (j>0  $\wedge$  R4=T<sub>14</sub><sup>j-1</sup>) }

r[] R4 T; { $\rightsquigarrow$  T<sub>14</sub><sup>j</sup>}

15: {R3=F1<sub>13</sub><sup>j</sup>  $\wedge$  R4=T<sub>14</sub><sup>j</sup>}

while R3  $\wedge$  R4 $\neq$ 2 {j<sub>end</sub>};

16: { $\neg$ F1<sub>13</sub><sup>j<sub>end</sub></sup>  $\vee$  T<sub>14</sub><sup>j<sub>end</sub></sup>=2}

skip (\* CS2 \*)

17: { $\neg$ F1<sub>13</sub><sup>j<sub>end</sub></sup>  $\vee$  T<sub>14</sub><sup>j<sub>end</sub></sup>=2}

w[] F2 false;

18: { $\neg$ F1<sub>13</sub><sup>j<sub>end</sub></sup>  $\vee$  T<sub>14</sub><sup>j<sub>end</sub></sup>=2}

# The calculational design of the verification conditions by abstract interpretation

# The induction principle

- Given an invariance specification  $S_{inv}$  find a **stronger inductive invariant**  $S_{ind}$
- Prove that  $S_{ind}$  satisfy verification conditions
  - Holds after initialization
  - Remains true after a computation step
  - Remains true after a communication
- Assuming  $S_{com} / H_{com}$

- Given an invariant  $I$  and a stronger inductive invariant  $I'$
- Prove that
  - Holds after one computation step
  - Remains true if  $I'$  holds
  - Remains true if  $I'$  holds
- Assuming  $I$  holds before a computation step

**Verification conditions =  
abstraction of the  
concrete  
transformer for  
one computation  
step**

# Calculational design of the verification conditions

$$\begin{aligned}
 & \alpha_{inv}(\alpha_{ana} \llbracket H_{com} \rrbracket (S^a \llbracket P \rrbracket)) \subseteq S_{inv} \\
 \Leftrightarrow & \alpha_{inv}(\{\xi \in S^a \llbracket P \rrbracket \mid S \llbracket H_{com} \rrbracket \xi = \text{allowed}\}) \subseteq S_{inv} \quad \{\text{def. } \alpha_{ana} \llbracket H_{com} \rrbracket \} \\
 \Leftrightarrow & \alpha_{inv}(S^a \llbracket P \rrbracket \cap \{\xi \in S^a \llbracket P \rrbracket \mid S \llbracket H_{com} \rrbracket \xi = \text{allowed}\}) \subseteq S_{inv} \quad \{\text{def. } \cap \} \\
 \Leftrightarrow & \alpha_{inv}(S^a \llbracket P \rrbracket) \cap \alpha_{inv}(\{\xi \in \Xi \mid S \llbracket H_{com} \rrbracket \xi = \text{allowed}\}) \subseteq S_{inv} \\
 & \quad \quad \quad \{\text{since } \alpha_{inv} \text{ preserves intersections}\} \\
 \Leftrightarrow & \alpha_{inv}(S^a \llbracket P \rrbracket) \dot{\cap} \alpha_{inv}(\alpha_{ana} \llbracket H_{com} \rrbracket (S^a \llbracket P \rrbracket)) \subseteq S_{inv} \quad \{\text{def. } \alpha_{ana} \llbracket H_{com} \rrbracket \} \\
 \Leftrightarrow & \exists S_{com} . \alpha_{inv}(S^a \llbracket P \rrbracket) \dot{\cap} S_{com} \subseteq S_{inv} \wedge \alpha_{inv}(\alpha_{ana} \llbracket H_{com} \rrbracket (S^a \llbracket P \rrbracket)) \subseteq S_{com} \\
 & \quad \quad \quad \{\Leftrightarrow\} \text{ For soundness, we have } \alpha_{inv}(S^a \llbracket P \rrbracket) \dot{\cap} \alpha_{inv}(\alpha_{ana} \llbracket H_{com} \rrbracket (S^a \llbracket P \rrbracket)) \\
 & \quad \quad \quad \subseteq \alpha_{inv}(S^a \llbracket P \rrbracket) \dot{\cap} S_{com} \subseteq S_{inv};
 \end{aligned}$$

( $\Rightarrow$ ) For completeness, we choose to describe exactly the communications that is  $S_{com} = \alpha_{inv}(\alpha_{ana} \llbracket H_{com} \rrbracket (S^a \llbracket P \rrbracket))$ .

$$\Leftrightarrow \exists S_{com} . (S_{com} \Rightarrow S_{inv}) \wedge (H_{com} \Rightarrow S_{com})$$

by defining the conditional invariance proof  $S_{com} \Rightarrow S_{inv}$  to be  $\alpha_{inv}(S^a \llbracket P \rrbracket) \dot{\cap} S_{com} \subseteq S_{inv}$  and the inclusion proof  $H_{com} \Rightarrow S_{com}$  to be  $\alpha_{inv}(\alpha_{ana} \llbracket H_{com} \rrbracket (S^a \llbracket P \rrbracket)) \subseteq S_{com}$ .

• • •  
 • • •  
 • • •

# Calculational design of the verification conditions

$$\begin{aligned}
 & \alpha_{inv}(\alpha_{ana}[[H_{com}]](S^a[[P]])) \subseteq S_{inv} \\
 \Leftrightarrow & \alpha_{inv}(\{\xi \in S^a[[P]] \mid S[[H_{com}]]\xi = \text{allowed}\}) \subseteq S_{inv} \quad \{\text{def. } \alpha_{ana}[[H_{com}]]\} \\
 \Leftrightarrow & \alpha_{inv}(S^a[[P]] \cap \{\xi \in S^a[[P]] \mid S[[H_{com}]]\xi = \text{allowed}\}) \subseteq S_{inv} \quad \{\text{def. } \cap\} \\
 \Leftrightarrow & \alpha_{inv}(S^a[[P]]) \cap \alpha_{inv}(\{\xi \in \Xi \mid S[[H_{com}]]\xi = \text{allowed}\}) \subseteq S_{inv}
 \end{aligned}$$

$$\Leftrightarrow \exists S_{com} \cdot (S_{com} \Rightarrow S_{inv}) \wedge (H_{com} \Rightarrow S_{com})$$

( $\Rightarrow$ ) For completeness, we choose to describe exactly the communications that is  $S_{com} = \alpha_{inv}(\alpha_{ana}[[H_{com}]](S^a[[P]]))$ .

$$\Leftrightarrow \exists S_{com} \cdot (S_{com} \Rightarrow S_{inv}) \wedge (H_{com} \Rightarrow S_{com})$$

by defining the conditional invariance proof  $S_{com} \Rightarrow S_{inv}$  to be  $\alpha_{inv}(S^a[[P]]) \cap S_{com} \subseteq S_{inv}$  and the inclusion proof  $H_{com} \Rightarrow S_{com}$  to be  $\alpha_{inv}(\alpha_{ana}[[H_{com}]](S^a[[P]])) \subseteq S_{com}$ .

...

...

...



# Verification conditions

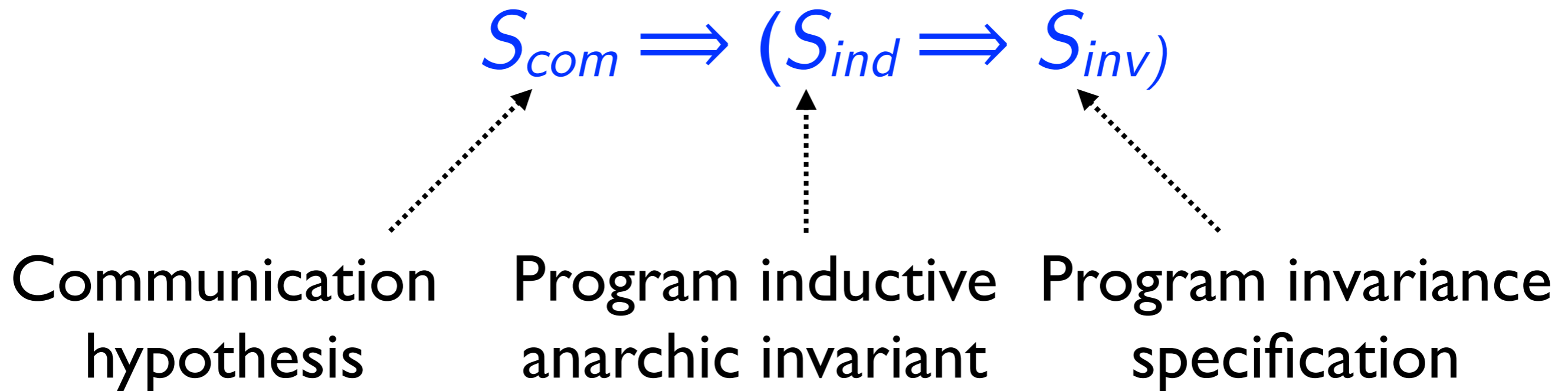
- Sequential proof
- Non-interference proof  
(like L/O-G but for different kind of invariants)
- Communication proof
  - a read event reading from a write event must be in **rf**
  - the value read for a variable is the one written
  - reading is fair in **rf** (cannot be delayed indefinitely)
  - ...

(useless in L/O-G since **rf** is fixed)

# The program consistency hypothesis $S_{com}$

# Communication hypothesis $S_{com}$

- A **sufficient communication hypothesis** can be discovered by calculational design:



- i.e.  $(S_{ind} \wedge \neg S_{inv}) \implies \neg S_{com}$
- Necessary: by counter examples

# Proving Consistency

$$\begin{array}{ccc} H_{com} & \Longrightarrow & S_{com} \\ \vdots & & \vdots \\ \text{cat} & & \text{invariant} \end{array}$$

# Proof method

- Obtained by calculational design:

$$\begin{aligned}
 & \alpha_{\text{inv}}(\alpha_{\text{ana}}[[H_{\text{com}}]](S^{\text{a}}[[\mathbb{P}]]) \dot{\subseteq} S_{\text{com}} \\
 \Leftrightarrow & \alpha_{\text{inv}}(S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P}) \dot{\subseteq} S_{\text{com}} && \{\text{def. } S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P}\} \\
 \Leftrightarrow & \forall \xi \in S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P} . \alpha_{\text{inv}}(\{\xi\}) \dot{\subseteq} S_{\text{com}} && \{\alpha_{\text{inv}} \text{ preserves } \cup\} \\
 \Leftrightarrow & \forall \xi \in S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P} . \bigcup_{p=1}^n \bigcup_{L \in \mathbb{P}_p} \{\alpha_{\text{inv}}(\xi')_p(L) \mid \xi' \in \{\xi\}\} \dot{\subseteq} S_{\text{com}} && \{\text{def. (19) of } \alpha_{\text{inv}}\} \\
 \Leftrightarrow & \forall (\tau_{\text{start}} \times \prod_{p=0}^{n-1} \tau_p \times \pi \times \text{rf}) \in S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P} . \forall p \in [1, n] . \forall L \in \mathbb{P}_p . \\
 & \alpha_{\text{inv}}(\tau_{\text{start}} \times \prod_{p=0} \tau_p \times \pi \times \text{rf})_p(L) \subseteq S_{\text{com}_p}(L) \\
 & \{\text{def. } \in, \dot{\cup}, \dot{\subseteq}, \text{ and } S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P} \text{ so that } \xi \text{ has the form } \xi = \\
 & \tau_{\text{start}} \times \prod_{p=0}^{n-1} \tau_p \times \pi \times \text{rf}. \text{ By def. (19) of } \alpha_{\text{inv}} \text{ and } \subseteq, \text{ we} \\
 & \text{get}\} \\
 \Leftrightarrow & \forall (\tau_{\text{start}} \times \prod_{p=0}^{n-1} \tau_p \times \pi \times \text{rf}) \in S^{\text{ana}}[[H_{\text{com}}]]\mathbb{P} . \forall i \in [1, n] . \forall L \in \mathbb{P}_p . \forall q \in [0, n[ . \forall k_q < |\tau_q| . \\
 & (\tau_q \downarrow_{k_q} = \mathfrak{s}\langle \kappa_{q,k_q}, \theta_{q,k_q}, \rho_{q,k_q}, \nu_{q,k_q} \rangle \wedge \kappa_{p,k_p} = L) \Rightarrow \\
 & \langle \kappa_{0,k_0}, \theta_{0,k_0}, \rho_{0,k_0}, \nu_{0,k_0}, \dots, \nu_{p-1,k_{p-1}}, \theta_{p,k_p}, \rho_{p,k_p}, \nu_{p,k_p}, \\
 & \kappa_{p+1,k_{p+1}}, \dots, \kappa_{n-1,k_{n-1}}, \theta_{n-1,k_{n-1}}, \rho_{n-1,k_{n-1}}, \nu_{n-1,k_{n-1}}, \text{rf} \rangle \\
 & \in S_{\text{com}_i}(L)
 \end{aligned}$$

# Proof method

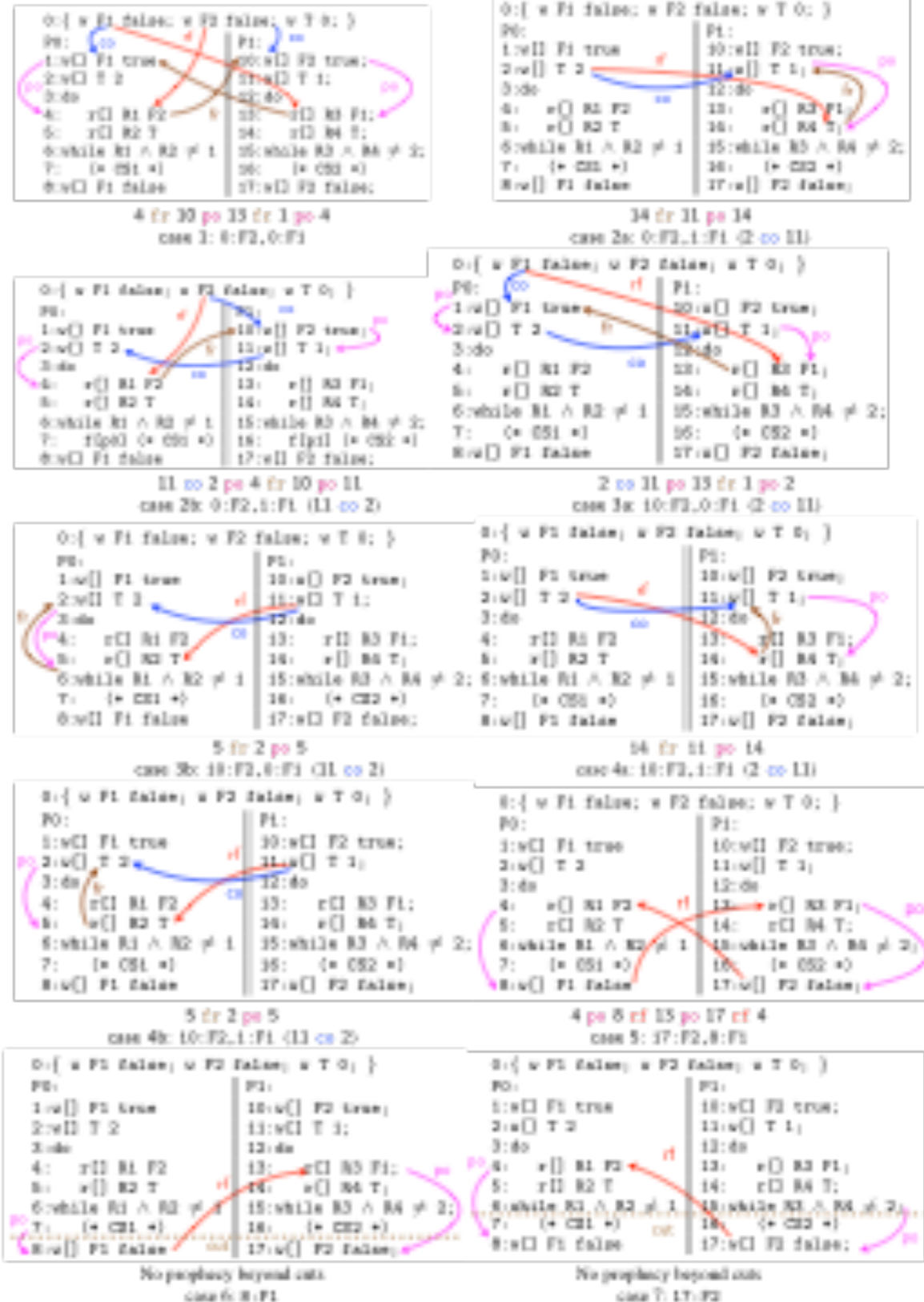
- The **anarchic invariants** can be used to calculate all communication **scenarios violating  $S_{com}$**
- These scenarios must be **forbidden by the cat specification  $H_{com}$**

(no need to reason at the level of traces of the anarchic semantics)

# Example (Peterson)

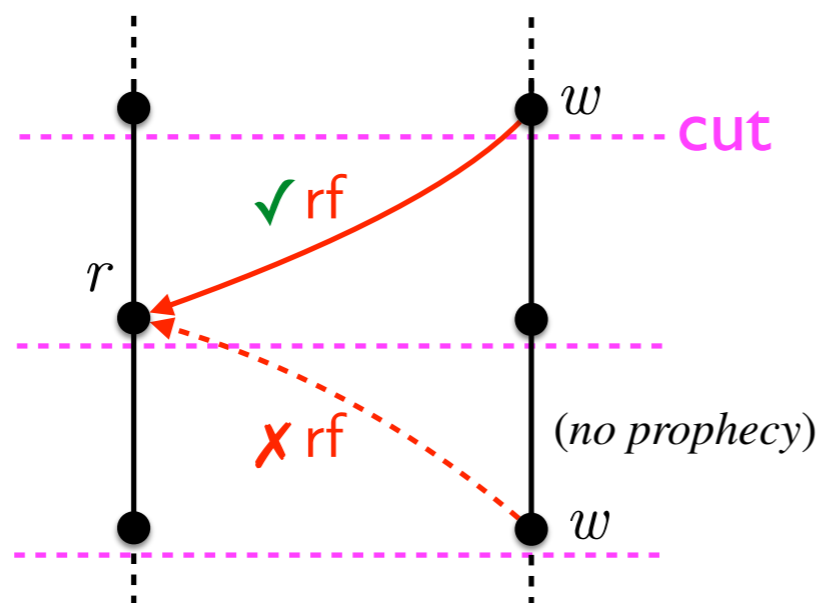
Communication scenarios violating  $S_{com}$  for Peterson

$$S_{com} \triangleq \neg[\exists i, j. [rf\langle F2_4^i, 0, false \rangle \vee rf\langle F2_4^i, 17, false \rangle \vee rf\langle T_5^i, 11, 1 \rangle] \wedge [rf\langle F1_{13}^j, 0, false \rangle \vee rf\langle F1_{13}^j, 8, false \rangle \vee rf\langle T_{14}^j, 2, 2 \rangle]]$$



# Incompleteness

- In general you have to add fences for  $H_{com}$  (do not change the invariants,  $S_{inv}$ ,  $S_{ind}$ , and  $S_{com}$  remain valid)
- $S_{com}$  can refer to communicated values not  $H_{com}$  in cat (redesign your algorithm without assuming that the hardware does know about communicated values)
- cat may not be expressive enough:



No read  
beyond cut



# Proving Architectural Consistency

$$M \implies H_{com}$$

⋮  
cat

⋮  
cat

$H_{com} \Rightarrow M \text{ in cat}$

- sound and complete proof method
- unpublished paper of JA and PC with Luc Maranget

# Beyond L/O-G: non-starvation

# Reasoning on one execution only

- A particular execution can be uniquely characterized by its read-from relation  $rf$
- We can reason on one execution only (Scm for this execution + Sind)
- Not directly possible with L/O-G
- Can be used to prove non-starvation

# Non-starvation (e.g. PostgrSQL)

- Consider **all traces that may starve** (for an appropriate  $S'_{com}$  for each trace)
- Prove each of them to be **infeasible**:
  - the inductive invariant  $S_{ind}$  under the program communication hypothesis  $S_{com}$  is unsatisfied
  - or, by strengthening the program communications  $S_{com}$  (maybe implemented by adding fences in  $H_{com}$ )
  - or, by a fairness hypothesis.

# Communication fairness hypothesis<sup>(\*)</sup>

- All writes eventually hit the memory:
  - If, at a cut of the execution, all the processes infinitely often write the same value  $v$  to a shared variable  $x$  and only that value  $v$
  - and from a later cut point of that execution, a process infinitely often repeats reads to that variable  $x$
  - then the reads will end up reading that value  $v$

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<sup>(\*)</sup> The SPARC Architecture Manual, Version 8, Section K2, p. 283: “if one processor does an  $S$ , and another processor repeatedly does  $L$ ’s to the same location, then there is an  $L$  that will be after the  $S$ ”.

# Conclusion

# Conclusion

- To **design** a correct parallel algorithm, specify:
  - the algorithm
  - the invariance specification  $S_{inv}$
  - the required program consistency model  $S_{com}$
- Find an **anarchic inductive invariant**  $S_{ind}$  satisfying the verification conditions such that  $(S_{com} \wedge S_{inv}) \implies S_{ind}$



# Conclusion

- To **implement** a parallel algorithm correctly:
  - Implement the program consistency model on an architecture consistency model  $M$  (possibly adding fences)
  - Prove  $M \Rightarrow S_{com}$
- Or better
  - Find a minimal/weakest  $H_{com}$  such that  $H_{com} \Rightarrow S_{com}$
  - $M \Rightarrow H_{com}$

# More work needed

- Specification of parallel/distributed program consistency models (more refined than architecture consistency models, e.g. cuts needed)
- Liveness (beyond non-starvation)
- Collection of certified algorithms for WCM (e.g. transactional memory, databases, etc)
- Static analysis (by abstract interpretation of the analytic semantics parameterized by a WCM)

# The End, Thank You