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<pre>1 Handout for CS 439 2 Class 9 3 12 February 2013 4 5 1. Implementing thm 6 7 Per-thread stat 8 9 typedef stm 10 unsigne 11 char *1 12 /* 13 }; 14 15 Machine-depende 16 17 void swtch 18 19 Machine-depende 20 21 void thread 22 23 Implementation 24 24 pushl %ebp 25 pushl %ebp 26 movl %(%ebg 29 movl 12(%eb 30 movl %esp, 31 movl (%eax 22 23 24 25 25 25 25 25 25 25 25 25 25 25 25 25</pre>	reads te in thread control block: ruct tcb { ed long esp; /* Stack po stack; /* Bottom co */ ent thread-switch function: (tcb *current, tcb *next); ent thread initialization fun d_init(tcb *t, void (*fn) (vc of swtch(current, next): ; movl %esp, %ebp ; pushl %esi; pushl %edi p),%eax (%edx)),%esp popl %esi; popl %ebx # Resto	<pre>inter of thread */ f thread's stack */ ction: id *), void *arg); # Save frame pointer # Save callee-saved regs # %edx = current # %eax = next # %edx->esp = %esp # %esp = %eax->esp</pre>	-	40 41 2. How can we impleted 42 2a. Here is A H 43 2a. Here is A H 44 45 struct Lock 46 int locked 47 } 48 void [BROKH 50 while (1) 51 if (lock 52 lock- 53 break 54 } 55 } 56 } 57 void release 58 void release 59 lock->loc 61 What's the 62 What's the 63 CPUs might 64 both will the 65 kind of rac 66 have made as 67 interleaving	<pre>ement locks, acquire(), and release()? BADLY BROKEN implementation: k { ed; EN] acquire(Lock *lock) {) { ck->locked == 0) { // C ->locked = 1; // D</pre>	on different D. Then the same th. But we co prevent

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70 2b. Here's a way th 72 some circumstan 73 use an atomic : 74 Use an atomic : 75 doing 76 "xchg a 77 does the follow 78 (i) freeze a: 80 (iii) temp = * 81 (iii) *addr = \$ 82 (iv) %eax = to	<pre>hat is correct but that is appropriate only hces: instruction on the CPU. For example, on the addr, %eax" wing: 11 CPUs' memory activity for address addr addr %eax emp e memory activity */ ddr, value) { 16; </pre>	in	129 130 2c. Here's ar 131 "threads" her 132 threads-insid 133 struct Mt 134 struct Mt 135 bool 136 threat 137 threat 138 Lock 139 } 140 141 142 143 144 The implet 145 acquit 146 while 147 mt	<pre>h object that does not involve busy waiting. re can be user-level threads, kernel threads be-kernel. The concept is the same in all content is_held; /* true if mutex held */ ad_id owner; /* thread holding mutex, ad_list waiters; /* queue of thread TCBs wait_lock; /* as in 2b */ ementation of acquire() and release() would ex_acquire(Mutex *m) { tre(&m->wait_lock); /* we spin to acquire (m->is_held) { /* someone else has the m->waiters.insert(current_thread) release(&m->wait_lock);</pre>	Note: the s, or cases. if locked */ */ be something like: wait_lock */ e mutex */
<pre>90 91 90 91 91 92 92 92 93 94 95 95 95 96 96 96 96 97 98 98 98 96 97 98 98 98 98 99 99 98 98 99 99 99 99 98 98</pre>	<pre>/* what does this do? */ al(&lock->locked, 1) == 0) n in acquire; call xchg_val() less frequent bck* lock) { g_val(&lock->locked, 1) == 1) { (lock->locked) ; </pre>	for s, g., if inning l what we se	149 5 150 7 151 8 152 m->is 153 m->ov 154 relea 155 9 156 1 157 void mute 158 acqui 159 acqui 160 m->is 161 m->ov 162 wake_ 163 relea 164 1 165 1 166 [Please I] 167 1 168 3. NOTE: the above 169 constraints on the 170 writes. For examp 171 How do we get the 172 they would not be 173 How do we get the 174 How do we get the 175 reordering, one m 176 fences (the "LFEN 180 not to re-order m 181 will not reorder 182 Moral of the abov 184 Terminology <td< td=""><td><pre>schedule(); /* run a thread that is on the acquire(&m->wait_lock); /* we spin again * s_held = true; /* we now hold the mutex mer = self; ase(&m->wait_lock); ex_release(Mutex *m) { tre(&m->wait_lock); /* we spin to acquire s_held = false; mer = 0; up_a_waiter(m->waiters); /* select and run ase(&m->wait_lock); tet me (MW) know if you see bugs in the above re mutex does the right thing only if there te order in which the CPU carries out memory ole, if operations _after_ mutex_acquire(); in other processor to happen in the opposite e protected by the lock, and the program wou e required guarantee? By ensuring that neith processor reorders instructions with respect swent reordering by the compiler, the program sust use special assembly instructions. For ICE*, "SFENCE", and "MFENCE" instructions, the instructions with respect to xchg() (and a re paragraphs: if you're implementing a conc the processor's documentation about how load dhow to enforce that the compiler *and* the reorder is which the compiler *and* the compiler *and* the reorder is which respect to xchg() (and a re paragraphs: if you're implementing a conc the more set the compiler *and* the compiler *and* the reorder is and the compiler *and* *and* the compiler *and* the compiler</pre></td><th><pre>// * // * wait_lock */ a waiter */ // a waiter */ // // // // // // // // // // // // /</pre></th></td<>	<pre>schedule(); /* run a thread that is on the acquire(&m->wait_lock); /* we spin again * s_held = true; /* we now hold the mutex mer = self; ase(&m->wait_lock); ex_release(Mutex *m) { tre(&m->wait_lock); /* we spin to acquire s_held = false; mer = 0; up_a_waiter(m->waiters); /* select and run ase(&m->wait_lock); tet me (MW) know if you see bugs in the above re mutex does the right thing only if there te order in which the CPU carries out memory ole, if operations _after_ mutex_acquire(); in other processor to happen in the opposite e protected by the lock, and the program wou e required guarantee? By ensuring that neith processor reorders instructions with respect swent reordering by the compiler, the program sust use special assembly instructions. For ICE*, "SFENCE", and "MFENCE" instructions, the instructions with respect to xchg() (and a re paragraphs: if you're implementing a conc the processor's documentation about how load dhow to enforce that the compiler *and* the reorder is which the compiler *and* the compiler *and* the reorder is which respect to xchg() (and a re paragraphs: if you're implementing a conc the more set the compiler *and* the compiler *and* the reorder is and the compiler *and* *and* the compiler *and* the compiler</pre>	<pre>// * // * wait_lock */ a waiter */ // a waiter */ // // // // // // // // // // // // /</pre>
			199 instructions, 200 is with a spi	ing that waiting queue with atomic hardware , as in 2c. The most natural way to "use the nlock, but there are others, such as turnir which works if we're on a single CPU machine	ng off