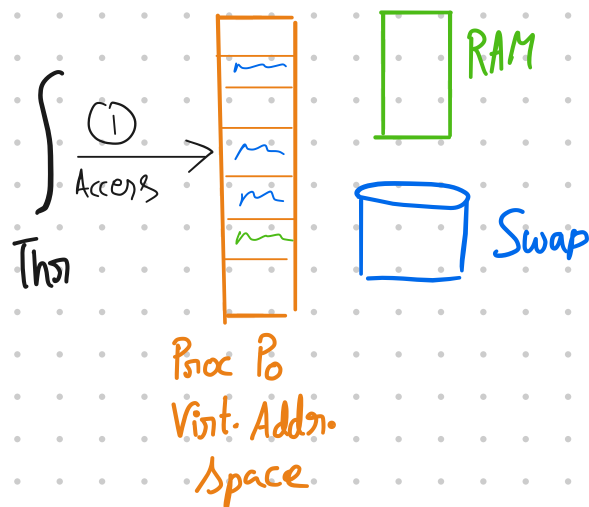


CS202 (002) Lec 14 - Virtual Memory

Last class

- Page faults $\leftrightarrow$ Demand paging



- Eviction policies: Might need to Evict, that is, move pages from RAM to swap to make space in physical memory.

Policy: What page to evict

Metric: Memory access time

p : Probability access handled by RAM

$$\begin{aligned} \text{Avg. time to access memory} &= p \cdot \frac{\text{time to access RAM}}{\sim 10-100\text{ns}} + (1-p) \cdot \frac{\text{time to access swap}}{\sim 1\mu\text{s} - 100\text{ms}} \\ &\quad 10^3\text{ns} \sim 10^8\text{ns} \end{aligned}$$

$\Rightarrow$ Minimize access from swap

- Belady's MIN (opt): Ideal policy - look into future to decide what to evict
 - +ve: Great perf
 - ve: Cannot be implemented

- Least Recently Used
 - Least Frequently Used
- Realistic (only requires observing past accesses)

Where we left off last class: how to implement?

- ① Maintain a data structure ordering pages by when they were last accessed (LRU) or access frequency (LFU)

Problem: Logic to maintain the data structure needs to run on every access
 ↳ Exception on every access

EXPENSIVE/BAD

We want hardware to help

x86-64 MMU (also other MMUs)

63	62	52	51	12	11	9	8	7	6	5	4	3	2	1	0
XD	Unused	Page physical base address				Unused	G		D	A	CD	WT	U/S	R/W	P=1
Available for OS (for example, if page location on disk)															P=0

Each entry references a 4K child page. Significant fields:

P: Child page is present in memory (1) or not (0)

R/W: Read-only or read-write access permission for this page

U/S: User or supervisor mode access

WT: Write-through or write-back cache policy for this page

A: Reference bit (set by MMU on reads and writes, cleared by software)

Reference Bit set to 1 when page is accessed.

NB: Kernel (or other software) responsible

D: Dirty bit (set by MMU on writes, cleared by software)

Page physical base address: 40 most significant bits of physical page address (forces pages to be 4KB aligned)

XD: Disable or enable instruction fetches from this page.

DIRTY

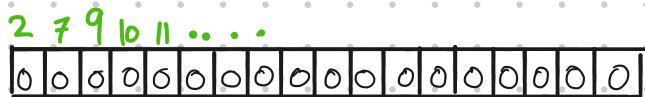
for setting it to 0

Bit set to 1 when page is modified (written to)

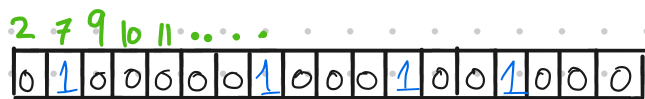
NB: kernel responsible for setting it to 0

What use is this

Reference Bits for
VPNs



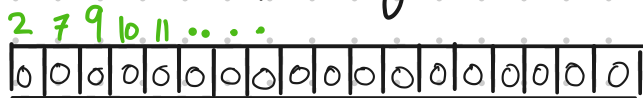
Program Executes



Kernel Updates



Cannot order them, but
were 'recently' accessed



$t=0$



Exception/
Timer interrupt/
... pauses
execution

Resume



Reference bit provides a way to determine what
pages were accessed "RECENTLY"
→ And with a bit more work, frequency.

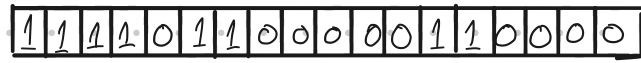
Using Reference Bit to approximate LRU - Clock

- Why? Popular algorithm implemented by many OS.

→ Low overhead

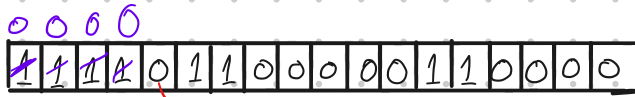
Core idea

Reference Bits



↑
clock hand

Exception &
Eviction necessary

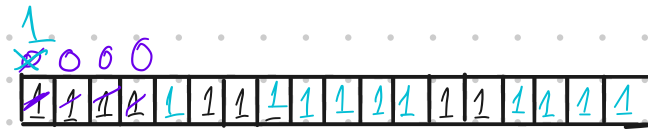


↑ → → → ↑

→ Evict this page

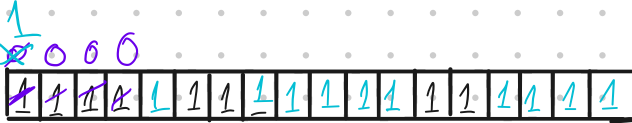
Resume

Time



↑ → → → ↑

Exc



↑ → → → ↑ → → → → → → → → → →

→ Evict this page.

How well does it approximate?

Time →

Access

		A	B	C	D	E	A	F	A	I
0	A	H					H		H	
1	B		H							
2	C			H						
3	D				H					

Eviction

LRO evicts?
B

4 E					H			
5 F							H	

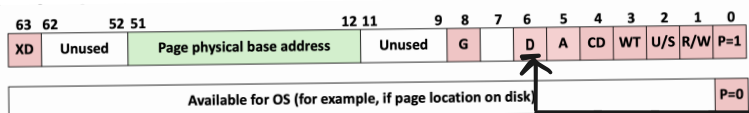
A

LP
B
Pac



Clock approximates $\angle RU$ using the access bit

- Aside:



Dirt

Page physical base address: 40 most significant bits of physical page address
(forces pages to be 4KB aligned)

XD: Disable or enable instruction fetches from this page.

Bit set to 1 when page is modified (written to)

NB: kernel responsible for setting it to $\emptyset$

Helps reduce eviction cost! How?

Other uses for Page Faults

- Copy on Write



— $\text{posk}()$ —→



2. 10. 111

0 75 10

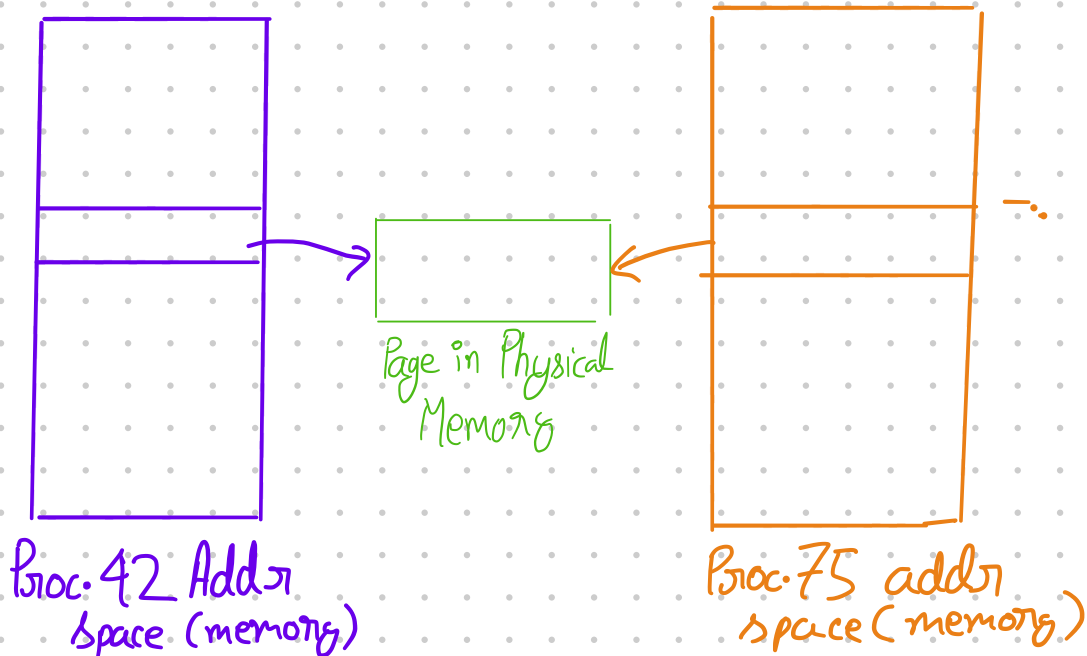
Proc. 42 Address
space (memory)

Proc. 75 address
space (memory)

- fork() :- Proc 42 & 75 should have the same memory content.

How? ① Make a copy
↳ Problem: Time

② Share pages?



Problem

```
1 int main(int argc, char* argv[]) {
2   int x = 4; ✓
3   if (fork() == 0) {
4     x *= 2; ←
5     printf("x = %d\n");
6   } else {
7     wait(NULL);
8     printf("x = %d\n", x); ←
9   }
10 }
```

x = 22;

Copy-On-Write

63	62	52	51	12	11	9	8	7	6	5	4	3	2	1	0
XD	Unused	Page physical base address				Unused	G		D	A	CD	WT	U/S	R/W	P=
Available for OS (for example, if page location on disk)															P=

Each entry references a 4K child page. Significant fields:

P: Child page is present in memory (1) or not (0)

U/S: Child page has read/write access permission for this page

∅: Read-only.

Writes cause

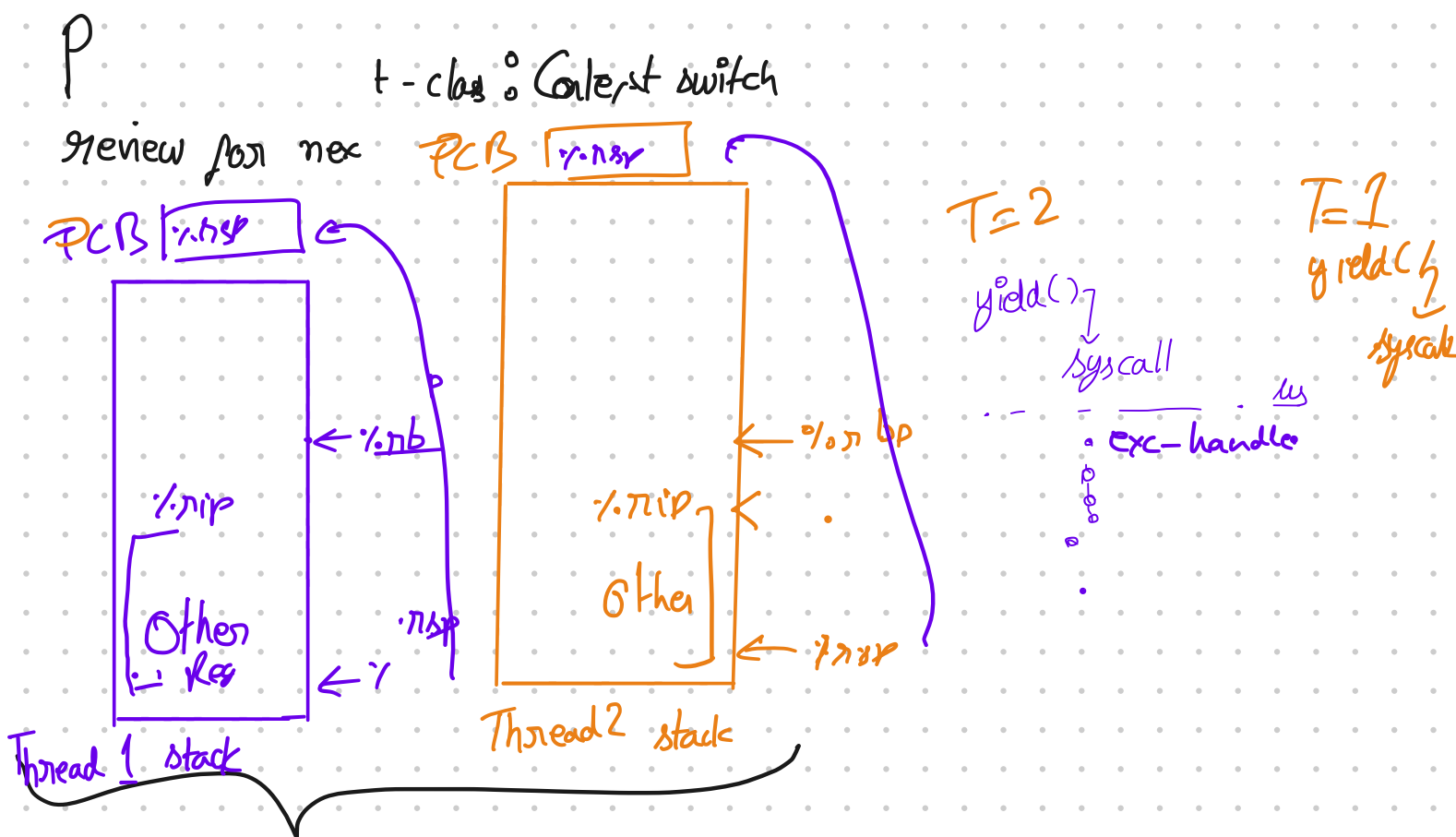
R/W: Read-only or read-write access permission for this page
 U/S: User or supervisor mode access
 WT: Write-through or write-back cache policy for this page
 A: Reference bit (set by MMU on reads and writes, cleared by software)
 D: Dirty bit (set by MMU on writes, cleared by software)
 Page physical base address: 40 most significant bits of physical page address
 (forces pages to be 4KB aligned)
 XD: Disable or enable instruction fetches from this page.

Writers
 a page-fault!

How can we use this?
 base addr
 0x2 {12
 offset

For each page what is
 the first offset that is
 accessed

- ① Pages already accessed
- ② Accessed address



Assume (for now) they are in the same process P

