Microprocessors

The MIPS Architecture
(System Level Instruction Set)
Mar 26th, 2002
Coprocessor 0 (System)

Load system control register
Store system control register
Read TLB entry
Store TLB entry
Write random TLB entry
Probe for matching TLB entry
Restore from Exception
The TLB

TLB = Translation Lookaside Buffer
Converts virtual to physical addresses
64 entries
- Entries 0-7 are “safe” (from random write)
- Entries 8-63 are freely addressable

Each entry maps one page
TLB Entry Format

VPN ➞ 20 bit virtual page number
- Pages are 4096 bytes
- So low order 12 bits are offset within page

PFN ➞ 20 bit physical page number

G ➞ flag indicating global page

PID ➞ Process ID
- Entry matches if VPN matches and either PID matches current process or G bit is set
Flag bits

- N = non-cacheable
- D = dirty
  - Indicates that the page has been modified, so must be written out to disk if it is removed
- V = valid
  - If not set, then this entry never matches
- G = global

No page by page protection

- Protection is done using address range
- 2 gigs for user, 2 gigs for system
Managing the TLB

If no matching TLB entry
- System trap is taken to specific trap routine
- This trap routine must readjust the TLB to contain the required entry, and then return to reexecute the load/store causing the trap
- Normal approach is to replace a random entry
  - No time to do anything more clever than this
  - Random register addresses random entry
  - Used to select entry to be clobbered
  - If entry is dirty, must be written first