FIGURE 4.15 The datapath of Figure 4.12 with all necessary multiplexors and all control lines identified. The control lines are shown in color. The ALU control block has also been added. The PC does not require a write control, since it is written once at the end of every clock cycle; the branch control logic determines whether it is written with the incremented PC or the branch target address. Copyright © 2009 Elsevier, Inc. All rights reserved.