Code Generation

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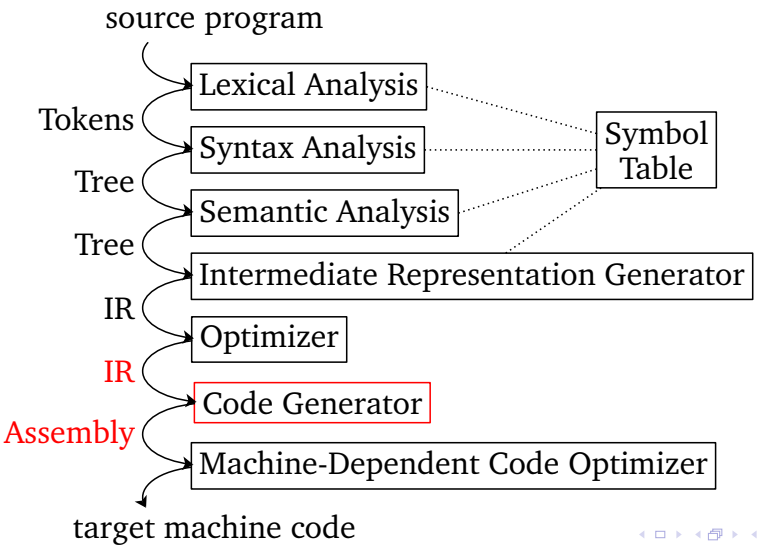
1. Issues
2. Target Language
3. Memory
4. Basic Blocks & Flow Graphs

Sixth compilation phase



1 Issues

2 Target Language

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What's Important?

- *Correctness*.
- Speed of target program.
- Speed of code generator.

Target Architectures

- CISC.
- RISC.
- Stack.

Only sequential architectures considered!

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Instruction Selection

- How closely does the IR match the target language?
- How good should the code be?
- What kind of architecture are we considering?

Example

```
a = b + c
d = a + e
```

```
LDR  r0,[sp,&B]
ADD  r0,r0,[sp,&C]
STR  r0,[sp,&A]
LDR  r0,[sp,&A]
ADD  r0,r0,[sp,&E]
STR  r0,[sp,&D]
```

Example

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a = b + c
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STR  r0,[sp,&D]
```

Example

```
a = b + c
d = a + e

LDR  r0,[sp,&B]     ;sp-relative OK when no local stack
ADD  r0,r0,[sp,&C]
STR  r0,[sp,&A]
LDR  r0,[sp,&A]
ADD  r0,r0,[sp,&E]
STR  r0,[sp,&D]
```

Register Allocation

- Hard!
- Operating system conventions.
- Hardware restrictions:
  - Special purpose registers (stack, index, frame, *etc.*)
  - Register pairs.
- Allocation—which variables are in registers?
- Assignment—which specific registers are used?

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ARM Machine Model

- Register machine with 13 general-purpose registers + sp/lr/pc.
- Load and store to byte-addressable memory.
- Computations.
- Jumps with optional return address save mechanism.
- Most operations may test and/or set condition codes.

Instruction (Sub)Set

```
MOV reg,arg             arg = #imm8 | reg | reg,LSL #imm5 | reg,LSR #imm5

ADD reg,reg1,arg2       reg = R0 | R1 | ... | R15 | SP | LR | PC
SUB reg,reg1,arg2
MUL reg,reg1,arg2       immn = n-bit constant

CMPS reg,arg

B   imm12
Bcd imm12               cd = EQ | NE | MI | PL | GE | LT | GT | LE
BL  imm12
                        b = B |
LDRb reg,mem
STRb reg,mem            mem = [reg,arg]
LDMFD reg!,mreg
STMFD reg!,mreg         mreg = { reg,...,reg }  (regs must be in order)
```

Load and Store

LDR r, mem Load: $r := *mem$.

STR r, mem Store: $*mem := r$.

where *mem* is one of

mem	Meaning
$[r, \&x]$	variable x in r frame
$[r, \pm r']$	char at $r \pm r'$
$[r, \pm r', shift]$	r'th member of array at r
$[r, \&x]!$	Same, with update

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mem	Meaning	C
$[r, \&x]$	variable x in r frame	`x`
$[r, \pm r']$	char at $r \pm r'$	`r[r']`
$[r, \pm r', shift]$	r'th member of array at r	`r[r']`
$[r, \&x]!$	Same, with update	`r[r'++]`

Instructions

$OP\ dst, reg_1, arg_2$	Operation: $dst := reg_1\ OP\ arg_2$.
$OP\ dst, reg$	Operation: $dst := OP(reg)$.
$\mathtt{B}\ L$	Jump: "goto" L.
$\mathtt{CMPS}\ reg_1, arg_2$	Compute $reg_1 - arg_2$, set $cond$.
$\mathtt{B}cond\ L$	Conditional jump: "if" $cond$ "goto" L; $cond \in \{\mathtt{MI}, \mathtt{PL}, \mathtt{LT}, \mathtt{GT}, \ldots\}$.

$x = y - z$

```
LDR  r1,[r11,&y]   // R1 = y
LDR  r2,[r11,&z]   // R2 = z
SUB  r1,r1,r2      // R1 = R1 - R2
STR  r1,[r11,&x]   // x = R1
```

$b = a[i]$

```
LDR r4,[r11,&i]         // r4 = i
ADD r5,r11,&a           // r5 = &a
LDR r6,[r5,r4,LSL#2]    // r6 = *(a+i)
STR r6,[r11,&b]         // b = R2
```

$a[j] = c$

```
LDR r4,[r11,&j]         // r4 = j
ADD r5,r11,&a           // r5 = &a
LDR r6,[r11,&c]         // r6 = c
STR r6,[r5,r4,LSL#2]    // *(a+i) = c
```

$*x = *y$

```
LDR r4,[r11,&y]     // r4 = y
LDR r5,[r4,#0]      // r5 = *y
LDR r6,[r11,&x]     // r6 = x
STR r5,[r6,#0]      // *x = *y
```

if $x < y$ goto L

```
LDR r4,[r11,&x]    // r4 = x
LDR r5,[r11,&y]    // r5 = y
CMPS r4,r5         // set flags from (x-y)
BLT  L              // if x<y goto L
```

Cost?

- Instruction size.
- Instruction memory accesses.
- Instruction execution time.

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Segments

Code	where the code is stored
Static	for constants that do not fit in instructions
Stack	for activation records with scoped values
Heap	for dynamically allocated and freed data objects

Calls

```
1    param 1;
2    param "Bar";
3    i = call foo;

4  ...

5  function int foo(int a, string b)
6  {
7    return a;
8  }
```

ARM Call and Return Code Example

```
Caller:
  MOV r0, #1
  MOV r1, &BAR
  BL Callee
```

```
Callee:
  STMFD sp!,{r4-r11,lr}
  LDMFD sp!,{r4-r11,pc}
```

Continue...

ARM Call and Return Code Example

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Caller:
  MOV r0, #1
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ARM Call and Return Code Example

```
Caller:
  MOV r0, #1
  MOV r1, &BAR
  BL Callee
  Continue...
```

```
Callee:
  MOV pc, lr
```

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Idea

1. Basic Blocks are maximal sequences of consecutive three-address instructions,
   1. the control flow can only enter through first instruction,
   2. all branch instructions leave the block
2. Flow Graph is the the graph with basic blocks as nodes and branches as directed edges

```
1)  i = 1
2)  j = 1
3)  t1 = 10 * i
4)  t2 = t1 + j
5)  t3 = 8 * t2
6)  t4 = t3 - 88
7)  a[t4] = 0.0
8)  j = j + 1
9)  if j <= 10 goto 3
10) i = i + 1
11) if i <= 10 goto 2
12) i = 1
13) t5 = i - 1
14) t6 = 88 * t5
15) a[t6] = 1.0
16) i = i + 1
17) if i <= 10 goto 13
```

Reconstruct Dragon Book Figure 8.9 on the blackboard from this.

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Next-Use

How many registers are needed inside a basic block?

Questions?