Given the following datapath:

1. Write the microinstructions required to do the following, similar to slides 52-57 in lecture 3 (optimize as much as you can):
   a. Fetch
   b. Addi R1, R2, 5 \ (i.e. R1 = R2 + 5)
   c. lw R5, offset(R6) \ (i.e. R5 = Memory[R6 + offset])
2. Will we benefit if we add a register to the second input of the ALU (i.e. AIR2)? Justify.
3. What happens if we remove MAR?
4. Wouldn’it be more beneficial if the memory subsystem is connected to one, or both, busses of the datapath?