Final Exam

Please answer questions 1 and 2 on this paper and put all other answers in the blue book.

1. True/False. Please circle the correct response.
   a. T  F In the C and assembly calling convention that we used for this class, arguments to a function call are pushed in reverse (i.e. right-to-left) order.
   b. T  F In C, for the expression \((x \mid \text{THE}\_\text{MASK})\), where \text{THE}\_\text{MASK} has at least one bit that is not zero, the result will be zero if all the bits of \(x\) are zero.
   c. T  F In x86 assembly, the instruction \text{mov eax, [ebp+12]} (or \text{movl 12 (%ebp), %eax} in AT&T syntax) will add 12 to the value contained in the ebp register in order to compute a memory address.
   d. T  F In x86 assembly on a 32-bit machine, the instruction \text{pop eax} adds 4 to the value of the esp register.
   e. T  F For a read operation on a direct-mapped cache, if the tag in the specified address matches the tag in the corresponding cache entry, then a cache hit results – no matter what the status of any other bit in the cache entry is.
   f. T  F In the NRU (not-recently-used) cache replacement algorithm that was used in the L1 cache in the class project, it was impossible for the reference bit of a cache entry to be 0 but the dirty bit to be 1.
   g. T  F The use of a write-through cache is slower than a write-back cache because, using a write-through cache, the CPU must wait until the data is written to main memory before proceeding with the next instruction.
   h. T  F A multiplexer uses \(N\) select lines to select from \(2^N\) input lines.
   i. T  F A 32-bit adder can be used for subtraction if each bit of the second operand is first sent through a (32-bit) \text{NOT} gate and the carry-in to the adder is set to 1.
   j. T  F In an unclocked latch, setting both the S and the R inputs to 0 will cause the output Q to retain its current value.

2. Write the number AB31 hex in binary: _______________________________.
   b. Write the number 73 decimal in hex: ______________ and in binary: ______________.
   c. \(\log_{16}G = \______________\).
   d. In order to access all bytes in a 64MB memory, an address must have at least _____ bits.

3. Write a C procedure, \text{int foo(int x)}, that returns the index of the most significant bit of \(x\) whose value is 1. For example, if bit 15 of \(x\) is the most significant bit of \(x\) whose value is 1, then \text{foo} should return 15. If no bits are 1, then \text{foo} should return -1.

(Please turn page over)
4. Write an x86 assembly procedure `bar` that takes two parameters, an integer `n` and a pointer `p` to an integer array (i.e. `p` is the address of the start of the array), and adds up the first `n` integers of the array and returns the result.

5. 
   a. In the class project, when running the code in `test_memory_subsystem.c`, the simulated cache performance was much worse when addresses were generated randomly than when sequences of consecutive addresses were generated. Why is that?
   
   b. On a 32-bit machine, suppose there is a 2MB, 2-way set associative cache with 16 words per cache line. Further, suppose that an instruction issues a memory address for loading a single byte from memory into a register. Indicate how the various bits of the address are used by the cache hardware to determine whether a cache hit has occurred and, if so, to return the requested byte.
   
   c. Suppose there is a computer with a memory hierarchy consisting of an L1 cache, an L2 cache, and main memory. Suppose further that an access to L2 cache or main memory reads or writes an entire cache line at a time, but an access to L1 cache reads or writes a single word at a time. If an instruction generates the address of a word in memory to load into a register, describe how the caches and main memory are accessed in order to retrieve the specified word. That is, describe every possible scenario (depending on a hit or miss at the various levels of the hierarchy).

6. 
   a. Build, from AND, OR, and NOT gates, a circuit that represents the two-bit “less-than” function. That is, it has two two-bit inputs, A and B, and a single one-bit output, R, such that R is true when A < B. [Hint: enumerate the possible inputs for which the output is true.]
   
   b. As you saw in class, a clocked latch is built from an unclocked latch as shown below. Why are flip-flops used for storing bits in a CPU rather than clocked latches?
   
   c. Build from gates, multiplexers, decoders, and/or adders (including 32-bit versions of each) a circuit that takes two 32-bit inputs, X and Y, and outputs the value of the larger of X and Y. That is, it computes the equivalent of the following C code:

   ```
   output = X > Y ? X : Y;
   ```