SRAMs: fast memory for caches

- "height": # of addressable locations
- "width": # of bits per location

E.g., 256K x 1: 256K 1-bit locations
32K x 8: 32K, 8-bit locations

- 18 address lines
- 1 output line
- 20 lines

15 address lines
8 input
8 output
31 lines

Modern SRAMs are "narrow": x1 or x4

2 READ, 1 WRITE
REGISTER FILE IMPLEMENTATION

Select
Read Register 1

Read Data 1

Read Data 2

Select read register 2

Write enable
Write select
32K x 8 SRAM: 15 bit address

- use top 9 bits to select 8 smaller SRAMs, producing 8 64-bit values
- use bottom 6 bits to multiplex further, choosing 1 bit of 64-bit value

1 bit per SRAM/mux

DRAMS

"dynamic" - has to be refreshed periodically - written back
- value is stored as a charge in a capacitor (transistor)
- slower, cheaper
- refresh happens automatically by memory controller
- two level decoding structure refreshes whole row at a time
- consumes 12-2% of available DRAM cycles (1987)