Some useful combinational building blocks:

**Decoder**

\[ \text{Nth output line is asserted when N is the value of the input} \]

\[ \text{out}_0 = \overline{\text{IN}} \]
\[ \text{out}_1 = \overline{\text{IN}} \]

Implement a 1-bit decoder

\[ \text{2-bit decoder} \]

\[ \text{out}_0 = \overline{\text{IN}_0} \cdot \overline{\text{IN}_1} \]
\[ \text{out}_1 = \overline{\text{IN}_0} \cdot \overline{\text{IN}_1} \]
\[ \text{out}_2 = \overline{\text{IN}_0} \cdot \text{IN}_1 \]
\[ \text{out}_3 = \text{IN}_0 \cdot \text{IN}_1 \]

**Multiplexer (aka MUX) - a selector**

Output gets the value of the \[2^{n-1}\] input \[2^n-1\] where \(N\) is the value of the selector.
Implementing a 2-input MAX

\[ \text{Out} = (\overline{IN0} \cdot S) + (\overline{IN1} \cdot S) \]

4 input MAX:

\[ \text{Out} = (\overline{IN0} \cdot \overline{S0} \cdot \overline{S1}) + (\overline{IN1} \cdot S0 \cdot \overline{S1}) + (\overline{IN2} \cdot S0 \cdot \overline{S1}) + (\overline{IN3} \cdot S0 \cdot S1) \]

Notice the common case of a "sum of products" where the only negation is on a variable or at the output.

- "two level logic"
- easily represented as a **programmable logic array (PLA)**
Clocks

- Need to indicate a change of state in sequential logic (i.e. storage logic)

- Regular change in voltage on a line

- Many circuits are edge triggered
  - Either rising or falling
  - Don’t have to be, but easiest to reason about.

All this to occur in a single cycle.
Memory Elements

basic elements are flip-flops & latches

clocked latch: simplest
\[ S-R = \text{set/reset} \]

\[ \begin{array}{c}
R \quad Q \\
S \quad \overline{Q}
\end{array} \]

- \( R=1, S=0 \rightarrow Q=1, \overline{Q}=0 \)
- \( S=1, R=0 \rightarrow Q=1, \overline{Q}=0 \)
- \( S=0, R=0 \rightarrow Q \text{ unchanged}, \overline{Q} \text{ unchanged} \)
- \( S=1, R=1 \rightarrow \text{ill defined} \) (unstable)

D latches & flip-flops

- clocked latch changes whenever inputs change & clock is asserted state.
- clocked flip-flop changes only upon a clock edge

- test only use clocked flip-flops
D Flip Flop w/ falling edge trigger

D must be asserted long enough so that correct value of Q is propagated from the first to the second latch.

D

C