Computer System Design
CSCI-GA2233-001

Lecture 1

Hubertus Franke
Course Administration

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• TextBook: Computer Organization and Design (4th edition)  
  Patterson & Hennessy (2008)  
  ISBN: 978-0-012-374493-7

• Class-URL: http://cs.nyu.edu/courses/fall11/CSCI-GA.2233-001/index.html

• Class-Material: posted after class on the website
Material Source

• Morgan Kaufman Slide Deck
• Occasional augmentation from slide deck of Mary Jane Irwin (PSU)
• And my own “stuff”
- Motivation
- Course Organization
- Administrative Stuff
From Intel 386 to Pentium 4

Intel 386, introduced 1985
275,000 transistors, 1 micron
16 MHz clock speed

Intel Pentium III, introduced 1999
9.5M transistors, 0.25 micron
600 MHz clock speed

Intel 4 Prescott, introduced late 04
125M transistors, 0.09 micron
2.8-3.8 GHz clock speed
Pentium III Microarchitecture

IFU: Instruction fetch unit
ID: Instruction dispatch
MIS: Micro-instruction sequencer
BTB: Branch target buffer
RAT: Register alias table
RS: Reservation station
IEU: Int. execution unit
FEU: FP execution unit
DCU: Data cache unit
ROB: Reorder Buffer
MOB: Memory Ordering Buffer
MIU: Mem Interface unit
Domain and Focus of Class

- Coordination of many Levels of Abstraction
- Underlying technology rapidly changing
Course Content and Goal

• **Content:**
  - Principles of computer architecture: CPU datapath and control unit design (single-issue pipelined, superscalar, VLIW), memory hierarchies and design, I/O organization and design, and introduction to advanced processor design (multiprocessors and SMT)

• **Course Goal:**
  - To learn the organizational paradigms that determine the capabilities and performance of computer systems. To understand the interactions between the computer’s architecture and its software so that future software designers (compiler writers, operating system designers, database programmers, …) can achieve the best cost-performance trade-offs and so that future architects understand the effects of their design choices on software applications.
This will make sense at the end of the class
Prerequisites

• Basic Logic Design and Machine organization
  – Bits, logic ..

• Able to run construct, compile, run and debug programs written in ‘C’ and assembly language

• Familiar with the Linux operating system and how to execute programs on it.
Course Organization/Structure

• Lectures (all approx).
  – 1 week review of basic architecture, performance principles.
  – 3 weeks MIPS ISA
  – 4 weeks pipelined datapath design issues and superscalar
  – 2 week memory hierarchies and memory design issues
  – 2 weeks I/O design issues
  – 1 week introduction to multiprocessor design issues
  – 1 week exams

• Assignments:
  – Generally homework assignments (1 hr)
  – Reading assignments (please follow the book)
  – Computer Design and Simulation Assignments
    • Building a simulator for a modern processor and evaluate various design choices
Grading

- **Class Participation:** 15%
  - This is a graduate class. *Participate*

- **Exams:**
  - Final Exam: 35%

- **Assignments:**
  - Homework: 20%
  - Programming/Labs: 30%
Todo’s

• Sign up for the class mailing list
  – See class website