Answer question 1 on this page. All other questions should be answered in the blue book.

1. **True/False.** Circle the appropriate choice.

   (a) **T**  **F** A TLB is simply a cache devoted to storing parts of a page table.
   (b) **T**  **F** The boolean terms \((a + b)\) and \((\overline{a} + \overline{b})\) are logically equivalent.
   (c) **T**  **F** If a datum is in the data cache, it can be accessed by a program without having a virtual address to physical address translation performed by the memory management hardware.
   (d) **T**  **F** The DMA controller generally serves as a bus master.
   (e) **T**  **F** In IEEE floating point arithmetic, it is possible for the addition of two non-zero numbers, \(N\) and \(M\), to result in \(N\).
   (f) **T**  **F** A 32-bit carry lookahead adder should be roughly twice as slow as a 16-bit carry lookahead adder.
   (g) **T**  **F** A 32-bit ripple adder should be roughly twice as slow as a 16-bit ripple adder.
   (h) **T**  **F** The number of stall cycles due to structural hazards occurring in a pipeline during program execution might be reduced by careful instruction scheduling by a compiler (i.e. by rearranging the order of instructions).
   (i) **T**  **F** Many pipelined processors contain a “popper”, a sharp instrument that pops pipeline bubbles when they arise.
   (j) **T**  **F** A 2-way set associative cache requires fewer gates to implement than a direct-mapped cache.

2. Figure 5.29 on page 372 of the text shows the single-cycle implementation of a simple MIPS processor that supports the jump instruction. Suppose you want to add support for the MIPS Jump-and-Link (JAL) instruction, such that

   \[ \text{JAL address} \]

   behaves exactly like the jump instruction except that the return address (i.e. the address of the next instruction) is saved in register 31.

   (a) Describe precisely how you would modify figure 5.29 to support JAL. If you want, you can draw the additional lines, devices, etc. that are needed (but you don’t have to).
   (b) Whether or not new Control output lines are needed, what value should be put on each Control output line when the processor is executing a JAL instruction?

3. (a) Draw the logic for a D flip-flop with a rising-edge trigger.
(b) Draw the two-level combinational logic, in “sum of products” form, that implements the following boolean equation:

\[ x = ((a \cdot \overline{b}) + (\overline{a} \cdot b)) \cdot c \]

Show how you arrived at your logic.

(c) Build a two-bit multiplier out of gates (i.e. it multiplies two two-bit numbers resulting in a 4-bit number).

4. Consider a machine with the following characteristics:

- 32-bit physical addresses
- 512KB, 8-way set associative cache
- cache line (block) size of 16 words

(a) Indicate how a 32-bit physical address would logically be partitioned into fields (byte offset, word offset, tag, etc). Be sure to indicate the size and position of each field in the address.

(b) Explain why set-associative caches might generally result in better performance than a direct-mapped caches.

(c) Write a simple piece of code (either C, Java, or Assembly) for which, when executed, you might expect to have a large number of conflict misses in the cache on the above machine.

(d) Assume that on the above machine, typical programs have a 96% cache hit rate for data, a 98% cache hit rate for instructions, and that 40% of instructions access memory (load/store). Suppose further that a cache miss costs 100 cycles. If the machine was upgraded so that it had the same processor, cache, and memory speed, but the cache was twice as big and had only 75% as many cache misses, how much faster would the upgraded machine run on typical programs?

5. Bus I/O

(a) Briefly explain why, when using a synchronous bus, the longer the bus is, the slower the bus clock must be.

(b) Figure 8.10 on page 661 of the text shows a handshaking protocol for reading one word from memory (assuming a 32-bit data bus) using an asynchronous bus. Suppose that the memory is able to, in response to a single read request, a return a block of 4 words (e.g. a 4-word cache line). Assuming the bus is still only 32-bits wide, draw (in the same way that figure 8.10 is drawn) the handshaking protocol for the block transfer situation.