These are practice exam questions for the material covered since the mid-term exam. Please note that the final exam is cumulative. See the practice mid-term exam questions for material from the first half of the course.

1. When performing signed division, the sign of the remainder should be the same as the sign of the dividend. Why?

2. Suppose there was a large floating point representation which used 16 bits for the exponent. If the exponent was represented using a bias, what would you expect the bias to be?

3. The following questions refer to figure 5.19 in Patterson & Hennessy.
   a. Why is the value of the PC register sent to an adder?
   b. With regard to the mux appearing to the left of the register file, under what circumstances is its control line ("RegDst") set to 0?
   c. Following the sign extend of bits 0-15 of an instruction, why is a "shift left 2" performed?
   d. Why are separate instruction and data memories required?
   e. What is the purpose of the and-gate connected to the "zero" output line of the ALU?
   f. If, in a given cycle, the value of the "read register 1" line of the register file is the same as the value of the "write register" line, what is to prevent the value on the "write data" line from being propagated immediately to the "read data 1" output line?

4. Figure 5.29 on page 372 of the text shows the simple, single-cycle datapath extended to implement a jump instruction. In order to accomplish this, another output line, the "jump" line, is added to the Control component. The opcode of a jump instruction is 2. Demonstrate how the Control should be extended by adding a new column to figure C.4 on page C-7 of the text, and by building a new Control out of gates, by extending figure C.5 on page C-8.

5. What are the characteristics of the MIPS Instruction Set Architecture (ISA) that facilitate pipelined execution?

6. The five stages of the simple MIPS pipeline we covered in class are: instruction fetch, instruction decode and register read, execute or calculate address, memory access, and register write. Describe the purpose of each of these stages.

7. Suppose a new, more complicated, instruction is desired for this simple pipelined MIPS processor. Suppose, also, it could be implemented by either
   (a) adding new logic to the execute stage of the pipeline, or
   (b) adding a new stage (i.e a 6th stage) altogether.
Assume that choice (a) would slow the execute stage down by 20%. Since choice (b)
increases the number of stages by 20%, is the overall effect on execution the same? If not, describe how each choice affects execution time and indicate which choice is better.

8. Define the terms "structural hazard", "control hazard", and "data hazard" in the context of pipelines. Which of these hazards is addressed by a hardware branch predictor (which guesses whether a branch will be taken or not)? For one of the other hazards, suggest a way, either in software or hardware, the effect of that hazard could be reduced.

9. Define the terms " spatial locality" and "temporal locality", and explain how caches are used to exploit them for a performance benefit. Be specific in the different ways that caches exploit these two phenomena.

10. Suppose physical addresses are 32 bits wide. Suppose there is a cache containing 256K words of data (not including tag bits), and each cache block contains 4 words. For each of the following cache configurations,  
     a. direct mapped  
     b. 2-way set associative  
     c. 4-way set associative  
     d. fully associative  
     specify how the 32-bit address would be partitioned. For example, for a direct mapped cache, you would need to specify which bits are used to select the cache entry and which bits are used to compare against the tag stored in the cache entry.

11. Draw the implementation of the 2-way set associative version of the above cache, at the level of detail shown in figure 7.19 on page 574 of the text. Be sure to include the logic for selecting the desired word of the cache block.

12. Cache misses can be characterized as one of the following: compulsory misses, capacity misses, and conflict misses. Describe how each of these kinds of misses can be addressed in the hardware.

13. Suppose you own a computer that exhibits the following properties on the programs that you run:  
    • the pipeline can accept a new instruction every cycle  
    • the cache can provide data every cycle (i.e. no penalty for cache hits)  
    • the instruction cache miss rate is 2.5%  
    • the data cache miss rate is 3.5%  
    • 30% of instructions are memory instructions  
    • the cache miss penalty is 80 cycles.
    
    Suppose, also, that you have decided to purchase a new computer. For the budget allocated, you can either  
    • purchase a machine with a processor and cache that is twice as fast as your current one (memory speed is the same as the old machine, though), or
• purchase a machine with a processor and cache that is the same speed as your old machine but in which the cache is twice as large.

Assume, for the purposes of this problem, that the cache miss rate for the programs you run will drop by 40% with this larger cache (although this is generally not true in the real world). Which computer are you best off purchasing? Explain in detail, showing the relative performance of each choice.

14. Describe the number of bits required in each entry of a TLB that has the following characteristics:
   • Virtual addresses are 32 bits wide
   • Physical addresses are 31 bits wide
   • The page size is 2K bytes
   • The TLB contains 16 entries of the page table
   • The TLB is direct-mapped